Magdy A. Bayoumi

The Center for Advanced Computer Studies (CACS)
University of Louisiana at Lafayette
301 East Lewis Street, ACTR Hall 201G, Lafayette, LA 70504-4330
OFFICE: Tel. (337) 482-6147; Fax (337) 482-5791
HOME: Tel. (337) 984-3330
Email: mab@cacs.louisiana.edu

I. Education

Ph.D., Electrical Engineering, University of Windsor, Canada, 1984
M.S., Computer Engineering, Washington University, St. Louis, 1981
M.S., Computer Science, Cairo University, Egypt, 1977
B.S., Electronics and Communications, Cairo University, Egypt, 1973

II. Research Interests

High Speed Networks and Multimedia Systems Architectures
VLSI Design, Methodology, and Architectures
Video and Image Processing Architectures
Digital Signal Processing Algorithms and Architectures
Neural Networks Algorithms and Architectures
Parallel Algorithms Design and Analysis

III. Teaching and Research Work at Universities

August 2007 - Present
Z.L. "Zeke" Loflin Eminent Scholar Endowed Chair in Computer Science, The Center for Advanced Computer Studies, University of Louisiana at Lafayette.

August 2000 - Present
Department Head, Computer Science Department, University of Louisiana at Lafayette (formerly, the University of Southwestern Louisiana).

August 2000 - August 2007
Alfred and Helen Lamson Endowed Professor of Computer Science, The Center for Advanced Computer Studies, University of Louisiana at Lafayette.

August 1998 - Present
Director, The Center for Advanced Computer Studies, University of Louisiana at Lafayette.

August 1997 - Present
Chair, CACS Board, The Center for Advanced Computer Studies, University of Louisiana at Lafayette.

March 1994 - August 2007
Edmiston Professor of Computer Engineering, The Center for Advanced Computer Studies, University of Louisiana at Lafayette.

August 1992 - February 1994

Professor of Computer Engineering, The Center for Advanced Computer Studies, University of Southwestern Louisiana. Established the SIMD Parallel Algorithms Prototyping Laboratory.

August 1987 - July 1992

Associate Professor of Computer Engineering, The Center for Advanced Computer Studies, University of Southwestern Louisiana. Established the Integrated Systems Design Laboratory.

August 1985 - July 1987

Assistant Professor of Computer Engineering, The Center for Advanced Computer Studies, University of Southwestern Louisiana. Established the VLSI Design Laboratory.

July 1982 - July 1985

Lecturer at the Department of Electrical Engineering, University of Windsor, Canada. Coordinator for the senior design project for two years. Conducted research in the areas of Digital Signal Processing, VLSI, and Microcomputer Applications. Also, participated in establishing a VLSI Design Center.

January 1982 - May 1984

Taught courses in Microprocessor Applications in the Department of Computer Science, University of Windsor. Developed an educational microcomputer laboratory.

IV. Courses Taught

VLSI Design (graduate and undergraduate)
VLSI Architecture (graduate)
VLSI Arrays (graduate)
Computer Arithmetic (graduate)
Digital System Verification (graduate)
VLSI Design Methodologies (graduate)
Digital and Image Signal Processing Architectures (graduate)
Application Specific Architectures (graduate)
ATM Architectures (graduate)
Video Signal Processing Architectures (graduate)
Microprocessors (undergraduate)
Logic Design (undergraduate)
Electronics (undergraduate)
Computer Architecture (undergraduate)

V. Honors

- In a formal ceremony, including ribbon cutting and dedication rituals, a VLSI Lab in a new College of Engineering in Hyderabad, India, was named after me: the Bayoumi Lab (Feb. 2006).
- Elected Vice President for Conferences, IEEE Circuits and Systems Society, 2006.
- IEEE Circuits & Systems Society 2003 Education Award, May 2003.
- United Nations Fellowship, TOKTEN Visitor, Egypt, 1994, 2002, 2003.
- French Government Fellowship, University of Paris IV Orsay, 1994, 1995, 2002.

- Chair, People-to-People Ambassador delegate to China, 2000.
- Fellow IEEE, 1999.
- Distinguished University Professor of the Year, 1993.
- USL Researcher of the Year, 1989.

VI. Department Activities

- Graduate Coordinator for Computer Engineering.
- CACS Executive Committee Member.
- Chairman, Research Committee (1992-1995).
- Co-Chairman, Colloquium Committee (until 1995).
- Co-Chairman, Admissions Committee.
- Co-Chairman, Financial Assistance Committee.
- Member, Graduate Studies Committee.
- Co-Chairman, Facilities Committee.

VII. University Activities

- Member, University Industrial Relations Committee (1996-1998).
- Member, Committee on Committees, 1995-present.
- President of Sigma Xi, USL Chapter (1991-1994).
- Co-coordinator (with Prof. Vijay Raghavan) for the Distinguished Lecture Series in VLSI Design and Applications 1991-1992.
- Coordinator for ‘‘VLSI Open House,’’ Feb. 28th, 1992, a one day program review by an out-of-state panel (from academia and industry); interested faculty members from all Louisiana Universities were invited.
- Member, University Graduate Council (1993-1996).
- Member, University Appeals Committee (1993-present).
- Member, USL Alumni Association, (1993-1995; 1996-1998).

VIII. State/Community Activities

- Member of Governor of Louisiana’s Commission on "Louisiana’s Comprehensive Energy Policy", 2002-2003.
- Advisory Board, Lafayette Economic Development Authority (LEDA).
- Board Member, International Trade Development Group, Le Centre International de Lafayette, 2001-present.
- Member, Chamber of Commerce.
  - Economic Development Committee
  - Education Committee
  - Technology Committee

- Vice-President, Lafayette Junior Leadership.

IX. Professional Activities (Selected)

National Committees

- NSF Panel in Networking, April 2004.
- NSF Panel in Nanotechnology, Feb. 2004.
- NSF Panel in Information Technology Research, Feb. 9-10, 2000.
- Vice President for Technical Activities, 1998 and 1999, IEEE Circuits and Systems Society.
- Elected to the IEEE Circuits and Systems Board of Governors (1996-2000).
- NSF panel in Instrumentation for Undergraduates, Washington, D.C., Jan., 1996.
- On the Advisory Board for the Project, ‘‘Special Education beyond year 2000,’’ US Department of Education (1990-1993); also serving on the Technology Panel for that project.
- On the Distinguished Visitor program for the IEEE Computer Society. (1991-1994).
- IEEE National Committee on Energy Policy, 1997 (representing the Circuits and Systems Society).
- IEEE National Committee on Communications and Information Policy, 1994 (representing the Circuits and Systems Society).
- IEEE National Committee on Engineering R&D Policy, 1994 (representing the Circuits and Systems Society).

Editorial Board

- Editor, VLSI Area, Microelectronic Encyclopedia, Academic Press (EIC: W.K. Chen).
- Associate Editor, IEEE Trans. on Circuits and Systems (1997-1999).
- Associate Editor, IEEE Trans. on Neural Networks (1994-1996).
- Associate Editor, IEEE Trans. on VLSI Systems (1995-1997).
- Regional Editor, Journal of VLSI Design.
- Associate Editor, INTEGRATION, The VLSI Journal.
- Associate Editor, Journal of VLSI Signal Processing.
- Advisory Board, Microelectronic Systems Integration Journal.
- Associate Editor, Journal of Circuits, Systems and Computers (1990-1996).
- Associate Editor of the IEEE Circuits and Devices Magazine (1989-1992).
- On the Editorial Board of the International Journal of VLSI Computer Aided Design (1989-1992).

Technical and Steering Committees

- Chair, VLSI Signal Processing Technical Committee of the IEEE Signal Processing Society, 2001-2003.
- Member, Multimedia Systems and Applications Technical Committee of the IEEE Circuits and Systems.

- Member, Neural Networks Technical Committee of the IEEE Circuits and Systems.
- Member, VLSI Systems and Applications Technical Committee of the IEEE Circuits and Systems, Past Chairman of the Committee (1989-1993); also a Founding Member of this Committee.
- Member, Steering Committee of the IEEE Midwest Symposium on Circuits and Systems.
- Secretary, VLSI Technical Committee of the IEEE Computer Society (1986-1988).
- Member, Steering Committee of the International Conference on Electronics, Circuits, and Systems (ICECS).
- Member, Steering Committee of the Workshop on Computer Architecture for Machine Perception (CAMP).

Conferences

- General Chair, *Ubiquitous Computing: Sensors and Wireless Sensor Networks Workshop*, December 29-30, 2008.
- General Chair, *IEEE International Symposium on Circuits and Systems (ISCAS 2007)*, May 27-30 2007, New Orleans, LA.
- Co-Program Chair, *IEEE Workshop on Signal Processing Systems (SiPS 2005)*, Nov. 2-4, 2005, Athens, Greece.
- International Program Committee Member, ConTEL, Zagreb, Croatia, June 15-17, 2005.
- Technical Program Committee, 11th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Tel-Aviv, Israel, Dec. 13-15, 2004.
- Technical Program Committee, 1st International Computer Engineering Conference (ICENCO'2004) New Technologies for the Information Society, Cairo, EGYPT, Dec. 27-30, 2004.
- General Chair, IEEE Computer Society Annual Symposium on VLSI, Feb. 19-20, 2004, Lafayette, LA.
- General Co-Chair, The 46th IEEE Midwest Symposium on Circuits and Systems, Dec. 2003, Cairo, Egypt.
- Publications Chair, IEEE Computer and Machine Perception, 2003.
- General Chair, 3rd International Workshop on Digital and Computational Video (DCV), Nov. 2002, Clearwater Beach, FL.
- General Chair, IEEE Workshop on Signal Processing Systems (SiPS), Oct. 11-13, 2000, Lafayette, LA.
- General Chair, 8th Great Lakes Symposium on VLSI, Feb. 19-21, 1998, Lafayette, LA.
- Member, Technical Program Committee of the IEEE Workshop on Signal Processing Design and Implementation.
- Member, Technical Program Committee of the International Symposium on Circuits and Systems (VLSI Track/Communication Track).
- Member, Technical Program Committee of the IEEE Great Lakes Workshop on VLSI, March, 1997, Urbana, Illinois.

- Member, Technical Program Committee of the International Conference on Computer Communications and Networks, Washington, D.C., Oct., 1996.
- Member, Technical Program Committee of the VLSI Signal Processing Workshop, San Francisco, Oct., 1996.
- International Liaison and Member of the Program Committee of the International Conference on Electronics, Circuits, and Systems (ICECS), Rodos, Greece, Oct., 1996, Chairman of a Session on CAD Systems.
- Member, Program Committee, The 9th International Conference on Parallel and Distributed Computing Systems, Dijon, France, 1996.
- Member, Technical Program Committee of the IEEE International Symposium on Circuits and Systems, Atlanta, May, 1996; Co-Organizer and Co-Chairman of the Special Session on Micromachining.
- Member, Technical Program Committee of the IEEE Midwest Symposium on Circuits and Systems (MWSCAS), Aug., 1996, Iowa.
- Chairman of a Session on DSP Architectures, 1996 Phoenix Conference on Computers and Communication.
- International Liaison and Member of the Program Committee of the International Conference on Electronics, Circuits, and Systems (ICECS), Amman, Jordan, Dec. 1995.
- Member, Panel on ‘‘Technology Transfer for Developing Countries,’’ ICECS, Dec. 1995.
- Member, Technical Program Committee of the Computer Architecture for Machine Perception, Como, Italy, Sept. 1995; Chairman of a Session on VLSI Architectures.
- Member, Technical Program Committee of the 38th Midwest Symposium on Circuits and Systems (MWSCAS), Rio de Janeiro, Brazil, Aug. 1995; Chairman of a Session on CAD Systems.
- Member, Technical Program Committee of the International Conference on Computer Communications and Networks, Las Vegas, Nevada, 1995.
- Member, Technical Program Committee of the VLSI Signal Processing Workshop, Japan, 1995; Chairman of a Session on VLSI Architectures.
- Member, Program Committee, The 8th International Conference on Parallel and Distributed Computing Systems, Orlando, Florida, 1995.
- Member, Program Committee, The 7th International Conference on Parallel and Distributed Computing Systems, Las Vegas, Nevada, 1994; Chairman of a Session on Parallel Applications.
- Member, Technical Program Committee of the VLSI Signal Processing Workshop, San Diego, 1994; (also served on the workshops of 1988-1993).
- Special Sessions Chairman, The First International Conference on Electronics, Circuits and Systems, Cairo, Egypt, Dec. 19-22, 1994.
- Member, Technical Program Committee of the IEEE Asia-Pacific Conference on Circuits and Systems, Taiwan, Dec. 5-8, 1994.
- Member, 12th International Conference on Pattern Recognition, Jerusalem, Israel, Oct. 1994.
- General Chairman, IEEE Midwest Symposium on Circuits and Systems, Aug. 1994.

- Program Committee, Third Workshop on Heterogeneous Computing, Cancun, Mexico, April 26, 1994.
- Special Sessions Chairman, Symposium on Intelligent Systems in Communications and Power, Puerto Rico, Feb. 1994.
- Co-chairman, VLSI Design Area of the technical program committee of the 1994 and 1993 IEEE International Symposium on Circuits and Systems (ISCAS); serving on the technical program committee since 1988.
- Co-Chairman, Computer Architecture for Machine Perception Workshop, New Orleans, Dec. 1993 (with Larry Davis, University of Maryland).
- Member, Technical Program Committee of the Computer Arithmetic Symposium, Windsor, Canada, June 1993.
- Organizer, Special Session ‘‘VLSI Architectures for DSP Applications,’’ IEEE Midwest Symposium on Circuits and Systems, Detroit, 1993.
- Member, Technical Program Committee of the IEEE Application Specific Array Processors, Aug. 1992.
- Organizer and Chairman of the special session on ‘‘Computer Arithmetic for DSP Applications,’’ IEEE Midwest Symposium, Washington D.C., Aug. 1992.
- Organizer, Workshop on Design Methodologies and Tools for DSP Architectures, ISCAS 92, Chicago, June 1992.
- Chairman of the first Louisiana Workshop on VLSI Research and Education, April 9-10th, 1992.
- Member, Technical Program Committee of the Computer Architecture for Machine Perception, Paris, France, Dec. 1991.
- Member, Technical Program Committee of the Computer Arithmetic Symposium, France, June 1991.
- Organizer and Chairman of the workshop on ‘‘Parallel Architectures and Algorithms for DSP Architectures,’’ ISCAS 91, Singapore, June 1991.
- Organizing and chairing many sessions in the past ten years in the following conferences: ISCAS, ICASSP, Midwest Symposium on Circuits and Systems, Asilomar Conference, the International Symposium on Parallel Processing, Computer Arithmetic Symposium, and the Workshop on Computer Architecture for Machine Perception.
- Serving on the program committee of Thirty-first International Symposium on Mini and Microcomputers and Their Applications, Austin, Texas, Nov. 10-12, 1986.
- Organizer and Reviewer for the Annual Modeling and Simulation Conference, Pittsburgh (1983-1985).

Guest Editor

- Co-Guest Editor, Special Issue on "Rapid Prototyping," European Journal on Signal Processing, 2002.
- Co-Guest Editor of the special issue, ‘‘Learning on Silicon,’’ Journal of Analog Integrated Circuits and Signal Processing, Kluwer, 1997.

- Guest Editor of the special issue, ‘‘Design Methodologies for VLSI Systems,’’ Journal of VLSI Signal Processing, Kluwer, 1994.
- Guest editor of the special issue, ‘‘VLSI Architectures for DSP Applications,’’ of the Circuits, Systems and Computers Journal, Dec. 1992.
- Guest Editor of the special issue on, ‘‘VLSI Design Methodologies for DSP Architectures,’’ of the International Journal of the VLSI CAD, July 1991.

Other Professional Activities

- ABET Program Evaluator
- Reviewer for the Computer Science Series, Mayfield Publishing Company (1983-1986).
- Referee for the following journals:
  * IEEE Transaction in Computers.
  * IEEE Transaction in Circuits and Systems.
  * IEEE Transaction in ASSP.
  * The International Journal of Mini Microcomputer.
  * Microcomputer Applications.
  * IEEE Expert.
  * Journal of Parallel and Distributed Computing.
- Reviewer for NSF.
- A principle advisor for the Laser Young Scholar Program; supervised a high school student during summer 1991 for Microelectronics training.

Professional Societies

- Fellow, IEEE.
- IEEE Computer Society.
- IEEE Circuits and Systems Society.
- IEEE ASSP Society.
- ACM SIGARCH (Special Interest Group on Computer Architecture).
- Mini and Microcomputer Society.
- A member of the executive committee of IEEE, Lafayette Chapter.
- A member of Sigma Xi Society.

X. Talks, Lectures, Short Courses and Workshops

- Distinguished Lecturer, ‘‘Wireless Sensor Networks: The Art of Integration,’’ Rice University Distinguished Lecture Series, January 15, 2009.
- Panelist, ‘‘Communication Advances for the Oil, Gas, and Energy Industries,’’ *IEEE Global Communications Conference (GLOBECOM) 2008*, December 3, 2008, New Orleans, LA.
- Keynote, ‘‘SoC: The Promise Land for Wireless Sensors Networks,’’ *International SoC Design Conference*, November 24, 2008, Busan, Korea.
- Invited Speaker, ‘‘Wireless Sensors Networks: Current and Future Challenges,’’ *University of Bridgeport, School of Engineering Colloquium Series*, November 13, 2008, Bridgeport, CT.

- Keynote Speaker, ''Wireless Sensor Networks: A Distributed Computing and Communication Paradigm,'' *21st International Conference on Parallel and Distributed Computing and Communication Systems (PDCCS-2008)*, September 24, 2008, New Orleans, LA.
- Plenary Speaker, ''Renewable Energy: From Intellectuality to Reality,'' *The 2nd IASTED International Conference on Power and Energy Systems*, September 9, 2008, Gaborone, Botswana.
- Panelist, ''Renewable Energy in Southern Africa,'' *The 2nd IASTED International Conference on Power and Energy Systems*, September 8, 2008, Gaborone, Botswana.
- Plenary Speaker, ''Wireless Sensor Networks,'' *IEEE International Conference on Circuits and Systems for Communications*, May 27, 2008, Shanghai.
- Invited Speaker, ''A Ubiquitous Computing and Monitoring System (UCoMS) for Oil Platforms Management,'' *IEEE International Conference on RFID 2008*, April 16, 2008, Las Vegas, Nevada.
- Keynote, ''New Wireless Sensors Networks: The Art of Integration,'' *14th IEEE International Conference on Electronics, Circuits and Systems*, December 12, 2007, Marrakech, Morocco.
- Keynote, ''Wireless Sensor Networks: A Collaborative and Embedded Information Processing Environment,'' *The 1st International Symposium on Information Electronics Systems*, November 27, 2007, Sendai, Japan.
- Keynote, ''Wireless Sensor Networks & DSP: Marriage Made in Heaven,'' *IEEE Workshop on Signal Processing Systems (SiPS 2007)*, October 17, 2007, Shanghai, China.
- Keynote, ''Wireless Sensor Networks: An Embedded Computing and Communication Paradigm,'' *The 4th International Forum of Digital TV & Wireless Multimedia Communication (IFTC 2007)*, October 16, 2007, Shanghai, China.
- Keynote, ''SoC: The Promise Land for Wireless Sensors Networks,'' *The 18th VLSI Design/CAD Symposium*, August 9, 2007, Taiwan.
- Invited Lecture, ''CACS' Role from Acadiana to Globalization,'' Lafayette Rotary Club, Holidome, August, 2007, Lafayette, LA.
- Keynote, ''Wireless Sensors Networks: Current and Future Challenges,'' *World Congress on Engineering (WCE 2007)*, July 2, 2007, Imperial College London.
- Opening Speech, ''Diversity is Unity,'' *International Week*, UL Lafayette, March 5, 2007, Lafayette, LA.
- Invited Speaker, ''Wireless Sensors Networks: the New Melting Pot,'' *IEEE Circuits and Systems Society Workshop, Spring 2007*, March 2, 2007, Vancouver, BC.
- Keynote, ''Renewable Energy: From Aristocracy and Intellectuality to Reality,'' *International Seminar on Renewable Energy*, January 29, 2007, Taipei, Taiwan.
- Invited Presentations (5 lectures) on ''Wireless Sensor Networks,'' Feb. 16-26, 2006, delivered to the following cities in India:
  - TI, Bangalore
  - Indian Institute of Science, Bangalore
  - IIT, Delhi
  - BITS, Pillani
  - CVR College, Hyderabad

- Plenary Talk, ‘‘Wireless Sensor Networks,’’ *IEEE Circuits and Systems Society, Workshop in New and Emerging Technologies*, March 20, 2006, Buenos Aires, Argentina.
- Keynote, ‘‘Wireless Sensor Networks: A New Life Paradigm,’’ *IEEE Circuits and Systems Workshop on ‘Engineering as Science’*, April 3-5, 2006, Bangkok, Thailand.
- ‘‘The World is Still Round,’’ Zydetech Monthly Meeting, Lafayette, LA, May 31, 2006.
- ‘‘Impact of Education on Community Advancement,’’ *19th International Sesame Exchange*, June 28-30, Vaasa, Finland.
- Keynote, ‘‘Wireless Sensor Networks: Present and Future Challenges,’’ *IEEE 3rd International Conference on Circuits and Systems for Comunications*, July 6-7, 2006, Bucharest, Romania.
- Invited Presentations (2 lectures), ‘‘Fundable Research Projects in Academia,’’ and ‘‘University Role in Technology Development and Commercialization,’’ *4th Conference on Scientific Research Outlook and Technology*, Dec. 10-15, 2006, Damascus, Syria.
- Keynote, ‘‘Wireless Sensor Networks: A New Life Paradigm,’’ *15th International Workshop - Power and Timing Modeling, Optimization and Simulation (PATMOS 2005)*, 20-23 September 2005, Leuven, Belgium.
- Plenary Talk, ‘‘Challenges and Opportunities of Silicon Technology in Communications,’’ *IEEE International Symposium on Signals, Circuits and Systems (ISSCS 2005)*, 14-15 July 2005, Iasi, Romania.
- Plenary Talk, ‘‘Wireless Sensor Networks: A New Communication Paradigm,’’ *7th IEEE Emerging Technologies Workshop: Circuits and Systems for 4G Mobile Wireless Communications (ETW 2005)*, 23-24 June 2005, St. Petersburg, Russia.
- Keynote, ‘‘Wireless Sensor Networks: A New Life Paradigm,’’ *IEEE International Northeast Workshop on Circuits and Systems (NEWCAS 2005)*, 19-22 June 2005, Quebec City, Canada.
- Plenary Talk, ‘‘Design of an Integrated RF-MEMS Based Wireless Signal Processor,’’ *IEEE International Northeast Workshop on Circuits and Systems (NEWCAS 2005)*, 19-22 June 2005, Quebec City, Canada.
- Keynote, ‘‘Wireless Sensor Networks: The Product of a Marriage Made in Heaven,’’ *IEEE International Conference on Telecommunications (ConTEL 2005)*, 15-17 June 2005, Zagreb, Croatia.
- Invited Talk, ‘‘Challenges and Opportunities of Silicon Technology in Communications,’’ 30 March 2005, Concordia University, Montreal, Quebec, Canada.
- ‘‘Challenges and Opportunities of Silicon Technology in Communications,’’ Plenary lecture at the *2nd IEEE International Conference on Circuits and Systems for Communications*, Moscow, Russia, June 30-July 2, 2004.
- ‘‘Wired or Wireless: It is the Silicon!’’ Keynote Speaker, *MELECON 2004*, Dubrovnik, Croatia, May 12-15, 2004.
- ‘‘INTEGRATION: Challenges and Opportunities,’’ VLSI Seminar Speaker, ATIPS Laboratory, University of Calgary, April 16, 2004.
- ‘‘Semiconductor Industry: Present and Future Challenges,’’ Developing Countries Microelectronics Workshop, Cairo, Egypt, Dec. 2003.
- ‘‘Low-Bit Rate Video Architectures,’’ National Electronic Research Institute, Cairo, Egypt, Jan. 2003.

- ‘‘Low-Power Video Architectures,’’ National Electronic Research Institute, Cairo, Egypt, July 2003.
- ‘‘Low Power Circuits and Architectures for Video Applications,’’ one-day Tutorial presented at Université de Montréal, May 19, 2000.
- Member of the Panel on, ‘‘VLSI Education: Present and Future,’’ the NSF VLSI Education Conference, July 1997, Washington, D.C.
- Member, Panel on ‘‘CAD Tools in Universities,’’ MWSCAS, Aug., 1996, Iowa.
- Many invited lectures nationally and internationally (1996-1999).
- ‘‘VLSI Research: An Architecture Perspective,’’ Intel, Inc., Oregon, Nov., 1996.
- ‘‘Technology Transfer from Academia to Small Business,’’ Mubark City for Applied Research, Alexandria, Egypt, July, 1996.
- ‘‘Application Specific Architectures for Video Signal Processing Applications,’’ University of Patras, Greece, June, 1996.
- ‘‘ATM Architectures for Multimedia Applications,’’ University of Paris, Orsay, Jan. 1996.
- ‘‘VLSI DSP Technology: Current and Future Technology,’’ Tufts University, March 1995.
- ‘‘Prototyping: An Evolving Technology,’’ University of Paris, Orsay, Jan. 1995.
- ‘‘Video Signal Processing Architectures,’’ University of Paris, Orsay, Jan. 1995.
- ‘‘VLSI DSP Technology: Current and Future Trends,’’ Cairo University (sponsored by the U.N. Tokton Program), Cairo, Dec. 1994.
- ‘‘Neural Architectures: A Hybrid Approach,’’ Egyptian National Microelectronic Institute (sponsored by the U.N. Tokton Program), Dec. 1994.
- ‘‘Video Signal Processing,’’ A Half Day Tutorial, Symposium on Intelligent Systems in Communications and Power, Puerto Rico, Feb. 1994.
- ‘‘VLSI DSP Technology: Current and Future Trends,’’ IEEE Computer Chapter and MCC, Austin, Dec. 1993.
- Invited Panelist, Panel on ‘‘Future of Application Specific Architectures,’’ Conference on Application Specific Array Processors, October 1993.
- ‘‘VLSI Education: A Hybrid Approach Between University and Commercial CAD Tools,’’ 36th Midwest Symposium on Circuits and Systems, August 1993.
- ‘‘Prototyping of Parallel Algorithms,’’ National Microelectronic Institute, Cairo, July 1993.
- ‘‘Hierarchical PetriNets for Modeling of Speed Independent Systems,’’ 1993 IEEE International Symposium on Circuits and Systems, May 3-6, 1993.
- ‘‘Microelectronics Technology: Present and Future,’’ IEEE Lafayette Chapter, Jan. 1993.
- ‘‘Design Methodologies for DSP Architectures,’’ Invited Distinguished Lecture, Department of Computer Engineering, King Fahd University for Petroleum and Minerals (KFUPM), Saudi Arabia, Dec. 1992.
- ‘‘An ASIC Chip for Image Segmentation,’’ Invited Distinguished Lecture, Department of Computer Engineering, King Fahd University for Petroleum and Minerals (KFUPM), Saudi Arabia, Dec. 1992.
- ‘‘VLSI Education: Present and Future,’’ Invited Distinguished Lecture, Department of Computer Engineering, King Fahd University for Petroleum and Minerals (KFUPM), Saudi

Arabia, Dec. 1992.

- ‘‘VLSI DSP Technology: Current and Future Trends,’’ Invited Distinguished Lecture, University of Riyadh, Saudi Arabia, Dec. 1992.
- ‘‘Parallel Algorithms for DSP Applications,’’ Dept. of Elec. Engg., University of Windsor, Aug. 1992.
- ‘‘Design Methodologies for VLSI DSP Architectures,’’ one day workshop, ISCAS, May 1992, San Diego.
- ‘‘VLSI DSP Technologies: Current and Future Developments,’’ IEEE Computer Chapter, Regina, Canada, April 1992.
- ‘‘A Parallel Paradigm for VLSI DSP Architectures,’’ IEEE Computer Chapter, University of Saskatewan, Saskatoon, Canada, April 1992.
- ‘‘VLSI DSP Technologies: Current Developments,’’ Manitoba IEEE Computer Society, April 1992.
- ‘‘VLSI DSP Architectures: Parallel Paradigm,’’ George Washington University Seminar Series, Feb. 1992.
- ‘‘Design Methodologies for DSP Architectures,’’ University of Santa Clara, Nov. 1991.
- ‘‘Parallel Algorithms for DSP Applications,’’ Tokyo Institute of Technology, Japan, 1991.
- ‘‘High Speed DSP Architectures,’’ Tokyo University, Japan, June 1991.
- Discussion on ‘‘Image Processing ASIC Architectures at USL,’’ NEC Inc., Japan, June 1991.
- Discussion on ‘‘VLSI Impact on the Massively Parallel Architectures,’’ Fujitsu Inc., June 1991.
- One day workshop on ‘‘Parallel Algorithms and Architectures for DSP Applications,’’ IEEE ISCAS, Singapore, June 1991.
- Distinguished Lecture on ‘‘Parallel Algorithms Prototyping,’’ Department of Computer Science, University of Saskatchewan, Canada, Nov. 1990.
- ‘‘An Image Segmentation ASIC Chip,’’ KAISTE, Seoul, Korea, Aug. 1990.
- One week Short Course on ‘‘VLSI-DSP: Current Developments and Future Trends,’’ Institute of Electronics and Center for Telecommunication Research, National Chiao Tung University, Taiwan, Aug. 1990.
- Tutorial on ‘‘Formal VLSI Design Methodologies,’’ Department of Electrical Engineering, University of Windsor, Canada, July 1989 (one week).
- Lecture on ‘‘What about Neural Computing,’’ Sigma XI Chapter, USL, 1989.
- Lecture on ‘‘VLSI Parallel Algorithms for Image Processing and Computer Vision,’’ Department of Elec. Engg., University of Southern California, Sept. 1989.
- Lecture on ‘‘VLSI Parallel Algorithms for DSP Applications,’’ The National Center for Microelectronics (ETRI), Korea, Sept. 1989.
- A keynote lecture on ‘‘VLSI Architectures for Image Processing and Computer Vision,’’ 1989 ROC Electron Devices and Materials Circuit Technology and Symposium (EDMS), Hsinchsu, Taiwan, Sept. 8-10, 1989.
- Tutorial on ‘‘VLSI Design Methods and Architectures,’’ Institute of Electronics and Center for Telecommunication Research, National Chiao Tung University, Taiwan, Sept. 1989.

- A keynote speech on ‘‘Neural Network Applications,’’ IEEE Houston Chapter, at Rice University, May 1989.
- ‘‘RNS Applications to VLSI; A System Approach to High Performance, Low Power, Dense Architectures for DSP,’’ Hughes, HMCTC in Carlsbad, California, June 1987.
- ‘‘Towards High-Speed Reliable VLSI Signal Processing Architectures,’’ GE Development and Corporate Center, Schenectady, Aug. 1987.
- ‘‘High Speed VLSI DSP Architectures Using Number Theoretic Transforms,’’ High Technology Center, Boeing Inc., Seattle, Aug. 1986.

XI. Student Supervisions

(A) Ph.D. Dissertations (and First Employment)

1. *Nam Ling,* ‘‘Systolic Temporal Arithmetic: A New Formalism for Specification, Verification, and Synthesis of Systolic Arrays,’’ Aug. 1989 (University of Santa Clara).
2. *Khaled Elleithy,* ‘‘A Formal Framework for High Level Synthesis of Digital Designs,’’ May 1990 (King Fahd University, Saudi Arabia).
3. *Ramakrishna N.A,* ‘‘A Design Methodology for the Synthesis of Application Specific Architectures,’’ May 1993 (California State University, Fresno).
4. *Aakash Tyagi,* ‘‘A Framework for Yield Modeling and Enhancement in Integrated Circuit Design and Fabrication,’’ May 1993 (Intel).
5. *Qutaibah Malluhi,* ‘‘Mapping Artificial Neural Networks on Massively Parallel Architectures,’’ (co-chair Dr. T.R.N. Rao), May 1994 (Jackson University).
6. *Bassem Alhalabi,* ‘‘A Hybrid Chip Set Architecture for Artificial Neural Network Systems with On-chip Learning and Refreshing,’’ May 1995 (Florida Atlantic Univ.).
7. *Majid Altuwaijri,* ‘‘A Parallel Recognition System for Arabic Cursive Words with Neural Learning Capabilities,’’ May 1995 (Saudi National Ministry).
8. *Rafic Ayoubi,* ‘‘Mesh-Based Neural Architectures,’’ Dec. 1995 (University of Balamand, Lebanon).
9. *Raghava Cherabuddi,* ‘‘A Design Methodology for Synthesis of Application Specific Multi-Chip Module Architectures,’’ Dec. 1995 (Intel, Santa Clara).
10. *Paul Shipley,* ‘‘VLSI Architectures for a New Class of ATM Switches,’’ May 1996 (Intel, Portland).
11. *Amr Elchouemi,* ‘‘An Explicit Rate Allocation Paradigm for Congestion Control in ATM Networks,’’ Dec. 1997 (Intel).
12. *Jimmy Limqueco,* ‘‘Fine-Grained and Course-Grained Architectures for 2-D Discrete Wavelet Transform,’’ May 1998 (Chips and Technology).
13. *Michael Weeks,* ‘‘Architectures for 3-D Discrete Wavelet Transform,’’ May 1998 (Georgia State University).
14. *Georgios Demetriou,* ‘‘A Hybrid Control Architecture for an Autonomous Underwater Vehicle (AUV)’’ May 1998 (University of Southern Mississippi).
15. *M. Al-Khatib,* ‘‘New Wireless ATM Automatic Error Control System,’’ May 1999 (University of South Alabama).

16. *Ashok Kumar,* ‘‘Multiple Voltage Based High Level Synthesis Methodologies for Low Power Design,’’ May 1999 (Cadence, Inc.).
17. *Beth Wilson,* ‘‘Texture Feature Extraction from the Wavelet Compressed Domain,’’ May 2000 (UL Lafayette).
18. *Ahmed Shams,* ‘‘High-Speed and Low-Power Architectures and Circuit Techniques for a Hybrid Mesh-based/Block-based Video Coder,’’ May 2000 (Intel).
19. *Wael Badawy,* ‘‘Low Cost Algorithms and VLSI Architectures for Object Based Digital Video Processing,’’ May 2000 (University of Calgary).
20. *Hanan Mahmoud,* ‘‘Low-Power Motion Estimation and Compensation Techniques for Low-Bit Rate Video Applications,’’ May 2001 (University of Alexandria).
21. *Ayman Fayed,* ‘‘Design and Analysis of Low-Power and Noise-Tolerant Multiply Accumulate Units,’’ May 2002 (Intel).
22. *Mohamed A.S. Elgamel,* ‘‘Interconnect Noise Analysis and Optimization for High-Performance Designs,’’ Dec. 2003 (University of Louisiana at Lafayette).
23. *Tarek Darwish,* ‘‘Energy Aware VLSI Design for MPEG Based Mobile Video Architectures,’’ Dec. 2003 (Intel).
24. *Archana Chidanandan,* ‘‘Decorrelator-based Parallel Interference Cancellation Receiver Architecture for the Base-station Receiver,’’ May 2004 (Rose-Hulman Institute of Technology).
25. *Mahmoud El-Assal,* ‘‘VLSI Architectures for Iterative Error Correcting Codes,’’ Dec. 2004 (Intel).
26. *Peiyi Zhao,* ‘‘Low Power, High Performance VLSI Circuits for Clocking System,’’ Dec. 2004 (Chapman University).
27. *Mathieu Kourouma,* ‘‘Mechanisms and Algorithms for Boosting Capacity in Personal Area Networks using Bluetooth Technology,’’ May 2005 (Southeastern Louisiana University).
28. *Walid Elgharbawy,* ‘‘Leakage Reduction and Subthreshold Operation in Nanometer CMOS Technologies,’’ Dec. 2005 (Intel).
29. *Rami El-Sayed Mohamed,* ‘‘Low-Power SRAM Design,’’ Dec. 2005 (Intel).
30. *Yijun Li,* ‘‘A System Platform for Image Transmission on Multi-hop Wireless Networks,’’ Dec. 2006 (Chrontel, Inc.).
31. *Sumeer Goel,* ‘‘A Smart Motion Estimation Paradigm for Real-Time Video Coding,’’ May 2007 (Cypress Semiconductor Corp.).
32. *Ruth M. Aguilar-Ponce,* ‘‘Automated Object Detection and Tracking Based on Clustered Sensor Network,’’ Dec. 2007 (State Univ. of San Luis Potosi, Mexico).
33. *Mitun Bhattacharyya,* ‘‘System Framework for Assessment and Reduction of Energy in Wireless Sensor Networks,’’ May 2008 (Sunmerge Systems, Inc.).
34. *Charbel J. Akl,* ‘‘Cost Effective Interconnect and Circuit Design Methods for High-Speed Nanometer CMOS VLSI Design,’’ December 2008 (Intel, Austin).
35. *Soumik Ghosh,* ‘‘The Design of ASPEN: An Asynchronous Sensor Processor for Energy Efficient Sensor Nodes,’’ December 2008 (University of Louisiana at Lafayette).
36. *Nan Wang,* ‘‘High Performance System-on-Chip Communication Architectures,’’ December 2008 (West Virginia Univ. Institute of Technology).

(B) M.S. Theses

1. Sanjay Popli, ‘‘Reliability and Yield Enchancement of Systolic Arrays,’’ May, 1988 (National Semiconductor, Santa Clara, CA).
2. Shantanu Gupta, ‘‘An On-line Testing Technique for Systolics,’’ May, 1988 (Intel Corporation, Hillsboro, OR).
3. Rajat Roy, ‘‘High Performance Bit-level Architecture for Real-time Digital Signal Processing’’ May, 1988 (AMD, Santa Clara, CA).
4. N. A. Ramakrishna, ‘‘Design of a CMOS Signal Processor for Fast Fourier Transforms,’’ May, 1988 (Stevens Institute of Technology).
5. Padma Akkiraju, ‘‘An Algorithm Specific VLSI Architecture for Kalman Filter,’’ May, 1990 (Cirrus Logic, San Jose, CA).
6. Subramanian Srinivasan, ‘‘VLSI Architecture for a Discrete Cosine Transform,’’ Dec., 1991 (Ross Technology, Austin, TX).
7. Srinivas Prasanna, ‘‘A Performance Driven Routing Methodology for Analog Circuits,’’ Dec., 1993 (Synopsys, CA).
8. Sachidanand Varadarajan, ‘‘An Area Efficient Technology Mapping for LUT Based FPGAs,’’ May, 1994 (Synopsys, CA).
9. Aditya Agrawal, ‘‘A Pre-emptive Congestion Control Scheme for a Shared Buffer ATM Switch,’’ May, 1995 (Level One, CA).
10. Anand Raju, ‘‘A VLSI Shared Multibuffer ATM Switch,’’ Dec., 1995 (Intel, Santa Clara).
11. Sausan Yazji, ‘‘Motion Estimation Architecture Based on Band-Matching,’’ May, 1997.

(C) M.S. Projects

Supervised more than 100 students working in the areas of: VLSI Architectures for DSP Applications, VLSI Design Methods, Fault Tolerance and Design for Testability, Parallel Algorithms and Architectures. These students are working in very respected and well established companies such as Sun Microsystems, AMD, Hewlett Packard Motorola, Intel, Cadence, MIPS, Actel, Cirrus Logic, Ross Technology, etc. Some of the projects are:

1. Harsha Krishnamurthy, ‘‘Clock Distribution for Low Power Architectures,’’ May, 1997.
2. Bassem Maaz, ‘‘Clock Distribution for Low Power MCM,’’ May, 1997.
3. Katta Maaz, ‘‘Low Power Design Methodology for FPGA Architectures,’’ May, 1997.
4. Sandeep Chaparala, ‘‘Low Power FPGA Design Methodology, May, 1997.
5. Ashok Kumar, ‘‘Low Power Logic Synthesis,’’ May, 1997.
6. Mangaparasard Gottam, ‘‘Low Power Architectures,’’ May, 1997.
7. Surendra Rajupalem, ‘‘Low Power MCM,’’ May, 1997.
8. Emad Y. Abu-Shama, ‘‘Low Power Adders,’’ Aug., 1996.
9. Michael Weeks, ‘‘ATM Architectures,’’ May, 1996.
10. Beth Lumetta, ‘‘Wavelet Architectures,’’ May, 1996.
11. Syed N. Quadri, Mohammed Osman, ‘‘DCT: A Complete Testable ASIC,’’ 1993.

12. Shaju Janardhanan, ‘‘Parameterized Hybrid Module Generators for Static and Dynamic Random Access Memories,’’ 1993.
13. Vinayak Gupta, ‘‘Module Generators for Storage Elements,’’ 1993 (Cypress Semiconductors, San Jose, CA).
14. Madhu Mannava, Madhav Kidambi, ‘‘Datapath Synthesis of Superpipelined Architectures,’’ Dec. 1993 (Cadence Design Systems, San Jose, CA, SMOS Inc, San Jose, CA).
15. A. Sivayya, ‘‘A Module Generation Environment for DSP ASICs in the Sphinx Design Framework,’’ Dec. 1991 (Ross Technology, Austin, TX).
16. E. Vasantha, ‘‘A Systolic Architecture for Two Dimensional DCT,’’ Aug. 1991 (Intel Corp, Portland, OR).
17. Elizabeth George, ‘‘A Systolic Architecture for Two Dimensional DCT,’’ Aug. 1991 (Chips and Technologies, CA).
18. Taher Madraswala, ‘‘A Load Balancing Approach towards Pipeline Scheduling in the Sphinx Design Framework,’’ Dec. 1991.
19. S. Thirumandas, ‘‘An Approach to Non-pipelined Synthesis,’’ Dec. 1990 (MIPS Inc. Sunnyvale, CA).
20. G. Hegde, ‘‘A Systolic Architecture for Median Filter,’’ May 1990 (LSI Logic, CA).
21. S. Myneni, ‘‘Design and Implementation of CMOS Cell Libraries for DSP Architectures,’’ May 1990 (Ross Technology, Austin, TX).
22. Sujana Sridharan, ‘‘Register and Bus Allocation using Weighted Cluster Partitioning,’’ July 1991.
23. Oscar Saldanha, ‘‘A Design Method of Bit-level DSP Architecture,’’ May 1989 (Cirrus Logic Inc).
24. Syn Hyan Chai, ‘‘Bit Level Architectures for IIR Filters,’’ May 1989.
25. H. Lai, ‘‘Reliable Modulo DSP Architectures,’’ May 1989.
26. M. Prasanna, ‘‘High Performance Butterfly Based on Quadratic Residue Number System,’’ May 1988; (started a computer company in Bangalore, India).
27. P. Nagendra, ‘‘A RISC Chip for Linear Transformation Algorithms,’’ May 1988 (Unisys, Los Angeles, CA).
28. Reddy Kosireddy, ‘‘A CMOS Neuron Based on the Schmitt Trigger,’’ May 1988 (Cirrus Logic Inc).
29. Hani M. Awajah, ‘‘A High Speed Modulo Decoder,’’ May 1988.
30. W. Bao, ‘‘A Systolic Architecture for Neural Nets,’’ Dec. 1988.

XII. Grants

(A) Principal Investigator and Co-Principal Investigator

- Principal Investigator, ‘‘Reconfigurable Complex DSP Systolic Arrays,’’ June 1988 - Dec. 1990, $59,497 (NSF).
- Principal Investigator, ‘‘An Integrated Digital Systems Design and Developments Laboratory,’’ June 1988 - May 1989, an enhancement grant of $453,000 (BOR of State of Louisiana).

- Principal Investigator, ‘‘VLSI Research and Education,’’ LaSER, (BOR of State of Louisiana) June 1991 - Dec. 1992, $29,264.
- Co-Principal Investigator, ‘‘A Research Program on Fault Tolerant Neural Networks,’’ NSF-Louisiana EPSCoR, Jan. 1992 - Dec. 1995, $2,420,000 (in a team lead by Prof. T.R.N. Rao).
- Principal Investigator, ‘‘Prototyping of Parallel Algorithms,’’ LEQSF (enhancement), $150,000, June 1992 - May 1993.
- Co-Principal Investigator, ‘‘VLSI Education for Louisiana,’’ LaSER, Jan. 1993 - Dec. 1994, $65,000 (with Dr. Gharavi from UNO).
- Co-Principal Investigator, ‘‘Classification and Avoidance in 3-D Underwater Automated Surveillance,’’ NSF, 1995-98, $250,717 (PI: Kimon Valavanis).
- Co-Principal Investigator, ‘‘Depend Activated Manufacturing Architecture (DAMA) Center Research Project,’’ DoE, 1995-97, $619,715 (PI: Al Steward).
- Principal Investigator, ‘‘Interoperable Underground Wavelet Transients Munitions Classification,’’ LEQSF (ITRS), $150,000, June 1, 1996 - June 30, 1999.
- Principal Investigator, ‘‘A Low Power Design Paradigm for Ultra Large Scale Integration Systems (ULSI),’’ DoE, July 1997 - Dec. 2003, $800,000.
- Principal Investigator, ‘‘Hardware Prototyping,’’ State of Louisiana, ITI Initiative, July 2001 - June 2006, $600,000.
- Co-Principal Investigator, ‘‘Scalable Routers,’’ State of Louisiana, ITI Initiative, July 2001 - June 2006, $1,727,000.
- Principal Investigator, ‘‘A Low Cost Video and Image Compression Framework,’’ NSF, July 2002 - August 2004, $46,940.
- Co-Investigator, ‘‘Ubiquitous Computing and Monitoring System (UCoMS) for Discovery and Management of Energy Resources,’’ DoE, June 2004 - May 2007, $1,200,000.
- Co-Investigator, ‘‘Ubiquitous Computing and Monitoring System (UCoMS) for Discovery and Management of Energy Resources,’’ BoR, State of Louisiana, June 2004 - May 2007, $1,200,000.
- Principal Investigator, ‘‘A Framework for Automated Scene Surveillance: Algorithms, Architecture, and Prototyping,’’ NSF, Aug. 2005 - Dec. 2007, $46,940.
- Principal Investigator, ‘‘Ubiquitous Computing with Sensors,’’ NSF, Aug. 2005 - Dec. 2007, $46,940.
- Principal Investigator, ‘‘CRI: MEMS Integration Infrastructure,’’ NSF, June 2006 - May 2008, $300,000.
- Principal Investigator, ‘‘Internet Tool Development and Web Site Maintenance in Support of Coastal Wetlands Restoration Activities in Louisiana,’’ USGS, Nov. 2006 - Oct. 2008, $55,000.
- Principal Investigator, ‘‘Sensor-Systems Design and Applications using high Performance Computing Resources,’’ Governor’s IT, July 2007 - June 2008, $99,443.
- Principal Investigator, ‘‘Scalable Middleware for Desktop Visualization for LITE Applications,’’ Governor’s IT, July 2007 - June 2008, $92,637.
- Principal Investigator, ‘‘Web-based Decision Support using Internet Tool to Provide Information and Data for Coastal Wetlands Restoration Activities,’’ USGS July 2007 - June

2009, $174,500.

- Principal Investigator, ‘‘U.S.-Egypt Workshop on Ubiquitous Computing: Sensors and Wireless Sensor Networks,’’ NSF, Oct. 2007 - Sept. 2008, $40,000.
- Principal Investigator, ‘‘Design of Smart Sensor and Its Implementation in Wireless Sensors Network,’’ NSF, Aug. 2007 - July 2009, $29,997.
- Co-Investigator, BoR, State of Louisiana, ‘‘Ubiquitous Computing and Monitoring System (UCoMS) for Discovery and Management of Energy Resources,’’ August 2007 - August 2010: $1,200,000 (State matching).
- ‘‘Sensor-Systems Design and Applications using high Performance Computing Resources,’’ Governor’s IT, July 2008 - June 2009, $100,000.
- ‘‘Scalable Middleware for Desktop Visualization for LITE Applications,’’ Governor’s ITI, July 2008 - June 2009, $100,000.
- Co-Investigator, DOE, EPSCoR, ‘‘Ubiquitous Computing and Monitoring System (UCoMS) for Discovery and Management of Energy Resources,’’ August 2007 - August 2010: $900,000.
- Co-Investigator, NSF, ‘‘MRI: Acquisition of a Wireless Nanonetowrks Integration and Emulation System for Multi-Processor SoC Research and Education,’’ August 2008 - August 2011: $500,000

(B) Investigator

- ‘‘Laboratory for Applied Artificial Intelligence,’’ LEQSF (enhancement), 1991-92, $60,000, with H. Chu, S. Dasgupta, C. Lursinsap, R. Loganantharaj, V. Raghavan.
- ‘‘Laboratory for Computer Vision and Multisensor Fusion Research,’’ LEQSF (enhancement), 1989-90, $130,000, with H. Chu, R. Loganantharaj, V. Raghavan, G. Seetharaman.

(C) Recruiting Grants

- Principal Investigator, ‘‘Graduate Fellowships in Computer Engineering,’’ Aug. 1991 - July 1996, $192,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Ph.D. Fellowships in Computer Engineering,’’ Aug. 1992 - July 1997, $128,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Superior Graduate Students in Computer Engineering,’’ Aug. 1993 - July 1998, $128,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Superior Graduate Students in Computer Engineering,’’ Aug. 1994 - July 1999, $64,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Superior Graduate Students in Computer Science,’’ Aug. 1996 - July 2001, $128,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Superior Graduate Students in Computer Science,’’ Aug. 1997 - July 2002, $136,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Graduate Fellows in Computer Science and Computer Engineering,’’ Aug. 1998 - July 2003, $68,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Graduate Fellows in Computer Science and Computer Engineering,’’ Aug. 1999 - July 2004, $136,000, LEQSF, State of Louisiana.

- Principal Investigator, ‘‘Recruitment of Graduate Fellows in Computer Science and Computer Engineering,’’ Aug. 2000 - July 2005, $64,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Graduate Fellows in Computer Science and Computer Engineering,’’ Aug. 2001 - July 2006, $64,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Graduate Fellows in Computer Engineering and Computer Science,’’ Aug. 2002 - July 2005, $58,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Recruitment of Graduate Fellows in Computer Science and Computer Engineering,’’ Aug. 2003 - July 2008, $72,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Assistance in the Implementation of Advanced Computer Technologies at the USGS NWRC Spatial Analysis Branch,’’ Jan. 2003 - Dec. 2005, $48,632, USGS.
- Principal Investigator, ’’Additional Assistance in the Development of Advanced Scientific Visualization Techniques for Display and Dissemination of High Resolution Geo-Spatial Imagery and Vector Datasets,’’ Sept. 2003 - June 2006, $33,410, USGS.
- Principal Investigator, ‘‘Recruitment of Graduate Fellows in Computer Science and Computer Engineering,’’ Aug. 2004 - July 2009, $72,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘‘Development of Advanced Scientific Vision-based Collection and Visualization Technique,’’ June 2005 - June 2007, $99,500, Corp. of Engineer.
- Principal Investigator, ‘Recruitment of Superior Graduate Students in Computer Science and Computer Engineering,’’ Aug. 2005 - July 2010, $80,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘Recruitment of Superior Graduate Students in Computer Science and Computer Engineering,’’ Aug. 2006 - July 2011, $176,000, LEQSF, State of Louisiana.
- Principal Investigator, ‘Recruitment of Superior Graduate Students in Computer Science and Computer Engineering,’’ Aug. 2007 - July 2012, $96,000, LEQSF, State of Louisiana.

XIII. Publications

(A) Books

- M. A. Elgamel and M. A. Bayoumi, ‘‘Interconnect Noise Optimization in Nanometer Technologies,’’ Book (Monograph), Springer 2006.
- G. Cauwenberghs and M.A. Bayoumi, ‘‘Learning on Silicon: Adaptive VLSI Neural Systems,’’ edited, Kluwer Academic Publishers, 1999.
- N. Ling and M.A. Bayoumi, ‘‘Specification and Verification of Systolic Arrays,’’ World Scientific, 1999.
- M.A. Bayoumi and E. Swartzlander, ‘‘VLSI Signal Processing Technology,’’ edited, Kluwer Academic Publishers, 1994.
- M.A. Bayoumi, ‘‘VLSI Design Methodologies for DSP Architectures,’’ edited, Kluwer Academic, 1993.
- M.A. Bayoumi, ‘‘Parallel Algorithms and Architectures for DSP Applications,’’ edited, Kluwer Academic Publishers, 1991.

(B) Proceedings

- IEEE Computer Society ‘‘Annual Symposium on VLSI,’’ Editors: A. Smailagic and M.A. Bayoumi, IEEE Press, 2004.
- ‘‘Third International Workshop on Digital and Computation Video,’’ Editor: M.A. Bayoumi, IEEE Press, 2002.
- ‘‘2000 IEEE Workshop on Signal Processing Systems, Design and Implementation,’’ Editors: M.A. Bayoumi, and E.G. Friedman, IEEE Press, 2000.
- ‘‘Eighth Great Lakes Symposium on VLSI,’’ Editors: M.A. Bayoumi, and G. Jullien, IEEE Press, 1998.
- ‘‘The 37th Midwest Symposium on Circuits and Systems,’’ Editors: M.A. Bayoumi, and K. Jenkins, IEEE Press, 1994.
- ‘‘Computer Architectures for Machine Perception,’’ Editors: M.A. Bayoumi, L. Davis, K. Valavanis, IEEE Computer Society Press, 1993.

(C) Book Chapters

- M. Bhattacharyya, Ashok Kumar, and M.A. Bayoumi, ‘‘Intelligent Mechanisms for Energy Reduction in Design of Wireless Sensor Networks using Learning Methods,’’ book chapter in *Integrated Intelligent Systems for Engineering Design*, IOS Press, Nov. 2006.
- •. R. Aguilar-Ponce, A. Kumar, J.-L. Tecpanectl-Xihuitl, and M.A. Bayoumi, ‘‘Automated Object Detection and Tracking for Intelligent Visual Surveillance based on Sensor Network,’’ book chapter, to appear in *Artificial Intelligence and Integrated Intelligent Information Systems: Emerging Techniques and Applications*, Idea-Group Press, 2006.
- •. M.A. Elgamel and M.A. Bayoumi, two chapters in *The Electrical Engineering Handbook*, Elsevier Academic Press, 2005.
- M. Elgamel and M.A. Bayoumi, ‘‘SoC Interconnect in Deep Submicron,’’ in *System-in-Chip for Real-Time Applications*, W. Badawy and G. Jullien (eds), Kluwer Academic Press, 2002.
- M.A. Bayoumi, ‘‘VLSI DSP Technologies: Current Developments,’’ VLSI Signal Processing Technology, M.A. Bayoumi and E. Swartzlander, Eds., Kluwer, 1994.
- M.A. Bayoumi and N.A. Ramakrishna, ‘‘Sphinx: A High Level Synthesis System for ASIC Design,’’ VLSI Design Methodologies, M. A. Bayoumi, Editor, Kluwer, 1993.
- N. Ling and M.A. Bayoumi, ‘‘A Formal Design Methodology for Systolic Arrays,’’ Transformational Approaches to Systolic Design, G.M. Megson (Ed), Springer-Verlag, 1992.
- N. Ling and M.A. Bayoumi, ‘‘Mapping Algorithms onto Multi-Dimensional Systolic Arrays,’’ *Progress in Computer Aided VLSI Design*, G.W. Zobrist (Ed), Ablex Publishing Co., 1990.

(D) Papers Published in Refereed Journals

2008

- C. Akl and M. Bayoumi, ‘‘Reducing Interconnect Delay Uncertainty via Hybrid Polarity Repeater Insertion,’’ *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 16, Issue 9, pp. 1230-1239, Sept. 2008.
- C. Akl and M. Bayoumi, ‘‘Transition Skew Coding for Global On-Chip Interconnect,’’ *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 16, Issue 8, pp. 1091-1096, Aug. 2008.

- C. Akl and M. Bayoumi, ‘‘Single-Phase SP-Domino: A Limited-Switching Dynamic Circuit Technique for Low-Power Wide Fan-in Logic Gates,’’ *IEEE Trans. Circuits and Systems-II (TCAS-II),* vol. 55, no. 2, pp. 141-145, Feb. 2008.

2007

- Walid M. Elgharbawy, Pradeep Golconda, Abdelhamid G. Moursy, and M.A. Bayoumi, ‘‘Novel Adaptive Body Biasing Techniques for Energy Efficient Subthreshold CMOS Circuits,’’ *Journal of Low Power Electronics JOLPE*, vol. 3, no. 2, pp. 175-188(14), Aug. 2007.
- Ramy E. Aly and M.A. Bayoumi, ‘‘Low-Power Cache Design Using 7T SRAM Cell,’’ *IEEE Transactions on Circuits and Systems II,* vol. 54, no. 4, pp. 318-322, April 2007.
- Peiyi Zhao, Jason McNeely, Pradeep Golconda, M.A. Bayoumi, Kuang W.D., and Bobby Barcenas, ‘‘Low Power Clock Branch Sharing Double-Edge Triggered Flip-Flop,’’ *IEEE Transactions on VLSI*, vol. 15, no. 3, pp. 338-345, March 2007.
- Nan Wang and M.A. Bayoumi, ‘‘System-on-chip Communication Architecture: Dynamic Parallel Fraction Control Bus Design and Test Methodologies,’’ *IET Proc. Computers and Digital Techniques Journal*, vol. 1, no. 1, pp. 1-8, Jan. 2007.

2006

- S. Goel, A. Kumar, and M.A. Bayoumi, ‘‘Design of Robust, Energy-efficient Full Adders for Deep Submicron Design Using Hybrid-CMOS Logic Style,’’ *IEEE Trans. on VLSI*, vol. 14, no. 12, pp. 1309-1321, Dec. 2006.
- Yijun Li and M.A. Bayoumi, ‘‘A Three-Level Parallel High-Speed Low-Power Architecture for EBCOT of JPEG 2000,’’ *IEEE Transactions on Circuits and Systems for Video Technology,* Sept. 2006.
- Yijun Li, Hongyi Wu, Nian-Feng Tzeng, Dmitri Perkins, and M.A. Bayoumi, ‘‘MAC-SCC: A Medium Access Control Protocol with Separate Control Channel for Reconfigurable Multi-hop Wireless Networks,’’ *IEEE Transactions on Wireless Communications*, July 2006.
- R. Aguilar-Ponce, Ashok Kumar, J.-L. Tecpanectl-Xihuitl, and M.A. Bayoumi, ‘‘A Network of Sensors Based Framework for Automated Visual Surveillance,’’ accepted, *Journal of Networks and Computer Applications*, Elsevier (scheduled publication in 2006).
- S. Goel, M. Elgamel, "M.A. Bayoumi," and Y. Hanafy, ‘‘Design Methodologies for High-performance Noise-tolerant XOR-XNOR Circuits,’’ *IEEE Trans. on Circuits and Systems I,* vol. 53, no. 4, pp. 867-878, April 2006.
- Ahmed Shams, Archana Chidanandan, Wendi Pan, and M.A. Bayoumi, ‘‘NEDA: a Low-power High-performance DCT Architecture,’’ *IEEE Transactions on Signal Processing*, March 2006.
- Mitun Bhattacharyya, Ashok Kumar, and M.A. Bayoumi, ‘‘Design and Analysis of Energy Reference Metric in a Cluster Based Wireless Sensor Network,’’ accepted for publication in *International Journal of Sensor Networks (IJSNet),* InderScience Publishers.

2005

- T. Darwish and M.A. Bayoumi, ‘‘Coefficient Elimination Algorithm for Low Energy Distributed Arithmetic DCT Architectures,’’ *Journal of VLSI Signal Processing*, vol. 40, pp. 355-369, 2005.
- R. Aguilar-Ponce, A. Kumar, J.-L. Tecpanectl-Xihuitl, and M.A. Bayoumi, ‘‘Autonomous Decentralized Systems based Approach to Object Detection in Sensor Clusters,’’ *IEICE*

Transactions on Communication Systems, IEICE/IEEE Joint Special Section on Autonomous Decentralized Systems, vol. E88-B, no. 12, pp. 4462-4469, Dec. 2005.

- A. Kumar and M.A. Bayoumi, ‘‘A Fast Scheduling Algorithm for Low Power Design,’’ *Journal of Circuits, Systems, and Computers, World Scientific,* Sept. 2005.
- Y. Li, H. Wu, N.-F. Tzeng, D. Perkins, and M.A. Bayoumi, ‘‘MAC-SCC: A Medium Access Control with a Separate Control Channel for Reconfigurable Multi-hop Wireless Networks,’’ *IEEE Transaction on Wireless Communications,* 2005.
- W. Elgharbawy and M.A. Bayoumi, ‘‘Leakage Sources and Possible Solutions in Nanometer CMOS Technologies,’’ *IEEE Circuits and Systems Magazine,* vol. 5, no. 4, pp. 6-17, Fourth Quarter 2005.
- M. Elgamel, Md I. Faisal, and M.A. Bayoumi, ‘‘Noise Metrics in Flip-Flop Designs,’’ *Special Issue on Recent Advances in Circuits and Systems, the Institute of Electronics, Information and Communication Engineers, IEICE, Transactions on Information and Systems,* vol. E88-D, pp. 1501-1505, July 2005.
- M.A. Bayoumi and Bertrand Zavidovique, ‘‘Special Issue on Prototyping for Machine Perception on a Chip,’’ *EURASIP Journal on Applied Signal Processing,* vol. 7, pp. 989-992, May 2005.
- M.A. Elgamel, A. Kumar, and M.A. Bayoumi, ‘‘Efficient Shield Insertion for Inductive Noise Reduction in Nanometer Technologies,’’ *IEEE Trans. on VLSI Systems,* vol. 13, no. 3, pp. 401-405, March 2005.

2004

- W. Badawy and M.A. Bayoumi, "A Low Power Architecture for HASM Motion Tracking," *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology,* vol. 37, no. 1, pp. 111-127, May 2004.
- P. Zhao, T.K. Darwish, M.A. Bayoumi, "High Performance and Low Power Conditional Discharge Flip-Flop," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 12, no. 5, pp. 477-484, May 2004.
- A. Kumar, M.A. Bayoumi, and M. Elgamel, ‘‘Methodology for Low Power Scheduling with Resources Operating at Multiple Voltages Source,’’ *Integration, The VLSI Journal* archive vol. 37, no. 1, pp. 29-62, Feb. 2004.

2003

- R.A. Ayoubi and M.A. Bayoumi, "Efficient Mapping Algorithm of Multilayer Neural Network on Torus Architecture," *IEEE Transactions on Parallel and Distributed Systems,* vol. 14, no. 9, pp. 932-943, Sept. 2003.
- M. Weeks and M.A. Bayoumi, "Discrete Wavelet Transform: Architectures, Design and Performance Issues," *Journal of VLSI Signal Processing,* vol. 35, no. 2, pp. 155-178, Sept. 2003.
- M.A. Elgamel and M.A. Bayoumi, "Interconnect Noise Analysis and Optimization in Deep Submicron Technology," *IEEE Circuits and Systems Magazine,* vol. 3, no. 4, pp. 6-17, Fourth Quarter 2003.
- B.A. Wilson and M.A. Bayoumi, "A Computational Kernel for Fast and Efficient Compressed-domain Calculations of Wavelet Subband Energies," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 50, no. 7, pp. 389-392, July 2003.

- P. Zhao, T. Darwish, and M.A. Bayoumi, "Low Power Conditional-Execution Pulsed Flip-Flop," *IEEE Computer Society, Looking Forward Magazine*, Summer 2003.
- W. Badawy, M. Talley, G. Zhang, M. Weeks, and M.A. Bayoumi, "Low Power Very Large Scale Integration Prototype for Three-dimensional Discrete Wavelet Transform Processor with Medical Applications," *The SPIE Journal on Electronic Imaging*, vol. 12, no. 2, pp. 270-277, April 2003.
- W. Badawy and M. Bayoumi, "A Parallel Multiplication-Free Algorithm and Architecture for Affine-based Motion Compensation," *The SPIE Journal on Optical Engineering*, vol. 42, no. 1, pp. 255-264, Jan. 2003.

2002

- M. Weeks and M.A. Bayoumi, ‘‘Three-dimensional Discrete Wavelet Transform Architectures,’’ *IEEE Transactions on Signal Processing*, vol. 50, no. 8, pp. 2050-2063, Aug. 2002.
- W. Badawy, M. Weeks, G. Zhang, M. Talley, and M.A. Bayoumi, ‘‘MRI Data Compression Using a 3-D Discrete Wavelet Transform,’’ *IEEE Engineering in Medicine and Biology Magazine*, vol. 21, no. 4, pp. 95-103, July-Aug. 2002.
- W. Badawy and M.A. Bayoumi, ‘‘A Low Power VLSI Architecture for Mesh-based Video Motion Tracking,’’ *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, pp. 488-504, July 2002.
- W. Badawy and M. Bayoumi, A Multiplication-Free Algorithm and A Parallel Architecture for Affine Transformation," *Journal of VLSI Signal Processing-Systems for Signal Image and Video Technology*, Kluwer Academic Publishers, vol. 31, no. 2, pp. 173-184, May 2002.
- W. Badawy and M.A. Bayoumi, ‘‘Algorithm-Based Low Power VLSI Architecture for 2d-Mesh Video Object Motion Tracking,’’ *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 12, no. 4, pp. 227-237, April 2002.
- A.M. Shams, T.K. Darwish, and M.A. Bayoumi, ‘‘Performance Analysis of Low-Power 1-bit CMOS Full Adder Cells,’’ *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 1, pp. 20-29, Feb. 2002.

2001

- M. Badawy, A. Kumar and M.A. Bayoumi, ‘‘A Co-design Methodology for High-Performance Real-time Systems,’’ the *Canadian Journal on Electrical and Computer Engineering*, vol. 26, pp. 141-146, July-Oct. 2001.

2000

- A. Shams and M.A. Bayoumi, ‘‘A Novel High-Performance CMOS 1-bit Full Adder Cell,’’ *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 5, pp. 478-481, May 2000.

1999

- M. Weeks, B. Wilson, and M.A. Bayoumi, "The Black Jack Tutor Chip: Dealing from Idea to Silicon," *IEEE Potentials*, vol. 18, no. 2, pp. 38-42, April-May 1999.

1998

- M.K. Kidambi, A. Tyagi, M.R. Madani, and M.A. Bayoumi, ‘‘Three Dimension Defect Sensitivity Modeling for Open Circuits in ULSI Structures,’’ *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 17, No. 4, pp. 366-371, April

1998.

- J.C. Limqueco and M.A. Bayoumi, ‘‘A VLSI Architecture for Separable 2D Discrete Wavelet Transform,’’ *Journal of VLSI Signal Processing*, vol. 18, pp. 125-140, 1998.
- M.M. Altuwaijri and M.A. Bayoumi, ‘‘A Thinning Algorithm for Arabic Characters Using ART2 Neural Networks,’’ *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 2, pp. 260-264, Feb. 1998.

1997

- R.A. Ayoubi, M.A. Bayoumi, A. Elchouemi and B. Alhalabi, ‘‘An Efficient Mapping Algorithm of Multilayer Perceptron on Mesh-Connected Architectures,’’ *Journal of Parallel Algorithms and Applications*, vol. 11, pp. 273-285, 1997.

1996

- R.A. Ayoubi, Q.M. Malluhi, and M.A. Bayoumi, ‘‘The Extended Cube Connected Cycles: An Efficient Interconnection for Massively Parallel Systems,’’ *IEEE Transactions on Computers*, vol. 45, no. 5, pp. 609-614, May, 1996.

1995

- K.M. Elleithy and M.A. Bayoumi, ‘‘A Systolic Architecture for Modulo Multiplication,’’ *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. II, pp. 725-729, Nov. 1995.
- Q.M. Malluhi, M.A. Bayoumi, and T.R.N. Rao, ‘‘Efficient Mapping of ANNs on Hypercube Massively Parallel Machines,’’ *IEEE Transactions on Computers*, vol. 44, no. 6, pp. 769-779, June 1995.
- Q. Malluhi, M.A. Bayoumi, and T.R. Rao, ‘‘Tree-Based Special Purpose Array Architectures for Neural Computing,’’ *Journal of VLSI Signal Processing*, vol. 11, pp. 245-262, 1995.

1994

- R. Ayoubi and M.A. Bayoumi, ‘‘Bitonic Sorting on Connection Machine,’’ *Journal of Parallel Algorithms and Applications*, vol. 3, pp. 151-161, 1994.
- A. Tyagi and M.A. Bayoumi, ‘‘The Nature of Defect Patterns on Integrated-Circuit Wafer Maps,’’ *IEEE Transactions on Reliability*, vol. 43, pp. 22-29, March 1994.
- Q.M. Malluhi and M.A. Bayoumi, ‘‘The Hierarchical Hypercube: A New Interconnection Topology for Massively Parallel Systems,’’ *IEEE Transactions on Parallel Processing*, vol. 5, no. 1, pp. 17-30, Jan. 1994.

1993

- M.M.A. Salama, H. Temraz, A.Y. Chikhani, and M.A. Bayoumi, ‘‘Fault-current Limiter with Thyristor-controlled Impedance,’’ *IEEE Transactions on Power Delivery*, vol. 8, no. 3, pp. 1518-1528, July 1993.

1992

- M.A. Bayoumi, P. Rao, B. Alhalabi, ‘‘VLSI Parallel Architecture for Kalman Filter: An Algorithm Specific Approach,’’ *VLSI Signal Processing Journal*, vol. 4, pp. 147-163, 1992.
- A. Tyagi and M.A. Bayoumi, ‘‘Image Segmentation on a 2D Array by a Directed Split and Merge Procedure,’’ in the *IEEE Transactions on Signal Processing*, vol. 40, no. 11, pp. 2804-2813, Nov. 1992.

- A. Tyagi and M.A. Bayoumi, ‘‘Defect Clustering Viewed through Generalized Poisson Distribution,’’ in the *IEEE Transactions on Semiconductor Manufacturing*, vol. 5, no. 3, pp. 196-206, Aug. 1992.
- K.M. Elleithy and M.A. Bayoumi, ‘‘Fast and Flexible Architectures for RNS Arithmetic Decoding,’’ *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 39, no. 4, pp. 226-235, April 1992.
- S. Popli, M.A. Bayoumi, A. Tyagi, ‘‘A Reconfigurable Technique for Reliable DSP Array Processors,’’ in the *Journal of Circuits, Systems and Computers*,’’ vol. 2, no. 3, pp. 281-304, 1992.

1991

- N. Ling and M.A. Bayoumi, ‘‘Formal Specification and Verification Strategies for Systolic Arrays,’’ *International Journal of Computer Aided VLSI Design*, pp. 91-112, 1991.
- K.M. Elleithy and M.A. Bayoumi, L.M. Delcambre, ‘‘VLSI Implementation of a Systolic Database Machine for Relational Algebra and Hashing,’’ *INTEGRATION, The VLSI Journal*, pp. 169-190, 1991.

1990

- N. Ling and M.A. Bayoumi, ‘‘Temporal Arithmetic: A New Formalism for Specification and Verification of Systolic Arrays,’’ *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 9, no. 8, pp. 804-820, Aug. 1990.
- Elleithy K.M. and M.A. Bayoumi, ‘‘A $\theta(1)$ Algorithm for Modulo Addition,’’ *IEEE Transactions on Circuits and Systems*, vol. 37, no. 5, pp. 628-631, May 1990.

1989

- M.A. Bayoumi and C.H. Yang, ‘‘Reconfigurable Testable Bit-Serial Multiplier for DSP Applications,’’ *IEE Proceedings*, vol. 136, no. 6, pp. 517-523, Nov. 1989.
- R. Roy and M.A. Bayoumi, ‘‘An Efficient Two’s Complement Systolic Multiplier for Real-Time Digital Signal Processing,’’ *IEEE Transactions on Circuits and Systems*, vol. 36, no. 11, pp. 1488-1493, Nov. 1989.
- M.M. Salama and M.A. Bayoumi, ‘‘A Microprocessor Based Testing Unit for Air-Core Power Reactor,’’ *The International Journal of Microcomputer Applications*, 1989.
- M.A. Bayoumi and N. Ling, ‘‘Testing of a NORA CMOS Serial-Parallel Multiplier,’’ *IEEE Journal of Solid-States Circuits*, vol. 24, no. 2, pp. 494-503, April 1989.
- N. Ling and M.A. Bayoumi, ‘‘Systematic Algorithm Mapping for Multi-Dimensional Systolic Arrays,’’ *Journal of Parallel and Distributed Computing*, vol. 1, no. 2, pp. 368-382, 1989.

1987

- N. Ling and M.A. Bayoumi, ‘‘An Efficient Technique to Improve NORA CMOS Testing,’’ *IEEE Transactions on Circuits and Systems*, vol. 34, no. 12, pp. 1609-1611, Dec. 1987.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Application,’’ *IEEE Transactions on Circuits and Systems*, vol. 34, no. 6, pp. 604-616, June 1987.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A VLSI Implementation of Residue Adders,’’ *IEEE Transactions on Circuits and Systems*, vol. 34, no. 3, pp. 284-288, March 1987.

1986

- M.A. Bayoumi, ‘‘Lower Bounds for VLSI Implementation of Residue Number System Architectures,’’ *Integration, VLSI Journal*, vol. 4, no. 4, pp. 263-269, Dec. 1986.
- M.A. Bayoumi and G.A. Jullien, ‘‘Analysis of Microprocessor Based Digital Filters,’’ *The International Journal of Mini and Microcomputers*, vol. 8, no. 3, pp. 56-60, 1986. Also, appeared in the *21st International Symposium on Mini and Microcomputers and their Applications*, pp. 52-56, May 1983.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘The Area-Time Complexity of a VLSI Digital Filter Using Residue Number Systems,’’ *Computers and Electrical Engineering, An International Journal*, vol. 12, no. 2, pp. 29-38, Feb. 1986.

1985

- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A Hybrid VLSI Architecture for FIR Filters using Residue Number Systems,’’ *Electronic Letters*, vol. 21, no. 8, pp. 358-359, April 1985.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A VLSI Implementation of Finite Impulse Response Digital Filters Using Residue Number Systems,’’ *Canadian Elect. Engg. Journal*, vol. 10, no. 2, pp. 76-80, April 1985.

1984

- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A VLSI Model for Residue Number System Architectures,’’ *Integration, The VLSI Journal*, vol. 2, no. 3, pp. 191-211, Sept. 1984.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘Multi Look Up Table Module for RNS Systems Implementation,’’ *Electronic Letters*, vol. 20, no. 1, pp. 94-95, Jan. 1984.

1983

- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘An Area-Time Efficient NMOS Adder,’’ *Integration, The VLSI Journal*, vol. 1, no. 4, pp. 317-334, 1983.

(E) Journal Papers Under Review and/or Revision

- H. Mahmoud, S. Goel, M. Shaaban and M.A. Bayoumi, "Multi-Stage Interval-Based Motion Estimation (MIME) Algorithm" to appear in *The Journal of VLSI Signal Processing Systems Kluwer Academic Publishers, 2nd Quarter 2004.*
- M.A. Elgamel, A.M. Shams, M.A. Bayoumi, and B. Zavidovique "Low Power Full Search Block Matching Motion Estimation VLSI Architectures," accepted and to appear in *Special issue on VLSI for Digital Video Processing in the Journal of Circuits, Systems and Computers.*

(F) Papers Published in Refereed Conferences

2008

- J. McNeely, Y. Ismail, M. Bayoumi, and P. Zhao, ‘‘Power Analysis of the Huffman Decoding Tree,’’ *IEEE International Conference on Image Processing (ICIP 2008)*, San Diego, CA, Oct. 12-15, 2008.
- C. Akl and M. Bayoumi, ‘‘Reducing Wakeup Latency and Energy of MTCMOS Circuits via Keeper Insertion,’’ *Intl. Symposium on Low Power Electronic Design (ISLPED)*, pp. 69-74, Aug. 2008.
- Md I. Faisal and M. Bayoumi, ‘‘A Low-Area, Low-Power Programmable Frequency Multiplier for DLL Based Clock Synthesizers,’’ *Proceedings of IEEE International*

Symposium on Circuits and Systems (ISCAS 2008), Seattle, WA, pp. 1460-1463, May 18-21, 2008.

- Y. Ismail, J. McNeely, M. Shaaban, M. Bayoumi, ‘‘A Generalized Fast Motion Estimation Algorithm using External and Internal Stop Search Techniques for H.264 Video Coding Standard,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2008)*, Seattle, WA, May 18-21, 2008.
- A. Moursy, I. Ajbar, D. Perkins, and M. Bayoumi, ‘‘Empirical Model-based Adaptive Control of MANETs,’’ *IEEE Workshop on Automated Network Management (ANM 2008)*, held in conjunction with IEEE INFOCOM, pp. 1-6, April 2008, Phoenix, AZ.
- C. Akl and M. Bayoumi, ‘‘Assumers for High-Speed Single and Multi-Cycle On-Chip Interconnect with Low Repeater Count,’’ *Great Lakes Symposium on VLSI (GLSVLSI08)*, pp. 327-332, May 2008.
- C. Akl and M. Bayoumi, ‘‘Cost-Effective and Low-Power Memory Address Bus Encodings,’’ *International Symposium on Circuits and Systems (ISCAS 2008)*, Volume, Issue 18-21, pp. 2010-2013, May 2008.
- C. Akl and M. Bayoumi, ‘‘Feedback-Switch Logic (FSL): a High-Speed Low-Power Differential Dynamic-Like Static CMOS Circuit Family,’’ *International Symposium on Quality Electronic Design (ISQED 2008)*, pp. 385-390, March 2008.
- C. Akl and M. Bayoumi, ‘‘Self-Sleep Buffer for Distributed MTCMOS Design,’’ *International Conference on VLSI Design (VLSID 2008)*, pp. 673-378, Jan. 2008.
- C. Akl and M. Bayoumi, ‘‘Wiring-Area Efficient Simultaneous Bidirectional Point-to-Point Link for Inter-Block On-Chip Signaling,’’ *International Conference on VLSI Design (VLSID)*, pp. 195-200, Jan. 2008.

2007

- Yasser Ismail, Mohamed Elgamel, and M.A. Bayoumi, ‘‘An Adaptive Block Size Phase Correlation Motion Estimation Using Smart Multireference Frames Selection In Frequency Domain,’’ *IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, Nov. 4-7, 2007.
- J.Luis Tecpanecatl-Xihuitl, Ruth M. Aguilar-Ponce, Yasser Ismail, and M.A. Bayoumi, ‘‘Efficient Multiplierless Polyphase FIR Filter based on New Distributed Arithmetic Architecture,’’ *IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, Nov. 4-7, 2007.
- Yasser Ismail, Mohamed Elgamel, and M.A. Bayoumi, ‘‘Adaptive Techniques for a Fast Frequency Domain Motion Estimation,’’ *IEEE Workshop on Signal Processing Systems (SiPS 07)*, Shanghai, China, pp. 331-336, Oct. 17-19, 2007.
- Nan Wang, Azeez Sanusi, Peiyi Zhao, Shaheen Mohamed, and M.A. Bayoumi, ‘‘PMCNOC: A Pipelining Multi-Channel Central Caching Network-on-Chip Communication Architecture Design,’’ *The IEEE Workshop on Signal Processing Systems (SiPS 07)*, Shanghai, China, pp. 487-492, Oct. 17-19, 2007.
- Jason McNeely and M.A. Bayoumi, ‘‘Low Power Lookup Tables for Huffman Decoding,’’ *IEEE International Conference on Image Processing (ICIP 2007)*, San Antonio, TX, vol. 6, pp. 465-468, Sept. 16-19, 2007.
- Yasser Ismail, Mohamed Elgamel, and M.A. Bayoumi, ‘‘A Fast Block-Based Motion Estimation Using Early Stop Search Techniques for H.264/AVC Standard,’’ *48th IEEE*

International Midwest Symposium on Circuits and Systems (MWSCAS 07)/NEWCAS, Montreal, Canada, Aug. 5-8, 2007.

- Abhijit Sil, Soumik Ghosh, and M.A. Bayoumi, ‘‘A Novel 8T SRAM Cell with Improved Read-SNM,’’ *48th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 07)/NEWCAS,* Montreal, Canada, Aug. 5-8, 2007.
- Yasser Ismail, Mohamed Elgamel, and M.A. Bayoumi, ‘‘Adaptive Techniques for a Fast Frequency Domain Motion Estimation,’’ *IEEE Workshop on Signal Processing Systems (SiPS 07),* Shanghai, China, pp. 331-336, Oct. 17-19, 2007.
- Nan Wang, Azeez Sanusi, Peiyi Zhao, Shaheen Mohamed, and M.A. Bayoumi, ‘‘PMCNOC: A Pipelining Multi-Channel Central Caching Network-on-Chip Communication Architecture Design,’’ *The IEEE Workshop on Signal Processing Systems (SiPS 07),* Shanghai, China, pp. 487-492, Oct. 17-19, 2007.
- Abhijit Sil, Soumik Ghosh, and M.A. Bayoumi, ‘‘A Novel 8T SRAM Cell with Improved Read-SNM,’’ *48th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 07)/NEWCAS,* Montreal, Canada, Aug. 5-8, 2007.
- Yasser Ismail, Mohamed Elgamel, and M.A. Bayoumi, ‘‘Adaptive Techniques for a Fast Frequency Domain Motion Estimation,’’ *IEEE Workshop on Signal Processing Systems (SiPS 07),* Shanghai, China, pp. 331-336, Oct. 17-19, 2007.
- Nan Wang, Azeez Sanusi, Peiyi Zhao, Shaheen Mohamed, and M.A. Bayoumi, ‘‘PMCNOC: A Pipelining Multi-Channel Central Caching Network-on-Chip Communication Architecture Design,’’ *The IEEE Workshop on Signal Processing Systems (SiPS 07),* Shanghai, China, pp. 487-492, Oct. 17-19, 2007.
- Jason McNeely and M.A. Bayoumi, ‘‘Low Power Lookup Tables for Huffman Decoding,’’ *IEEE International Conference on Image Processing (ICIP 2007),* San Antonio, TX, vol. 6, pp. 465-468, Sept. 16-19, 2007.
- Sherine AbdelHak, Abhijit Sil, Yi Wang, and M.A. Bayoumi, ‘‘Reducing Misprediction Penalty in the Branch Target Buffer,’’ *48th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 07)/NEWCAS,* Montreal, Canada, Aug. 5-8, 2007.
- Yasser Ismail, Mohamed Elgamel, and M.A. Bayoumi, ‘‘A Fast Block-Based Motion Estimation Using Early Stop Search Techniques for H.264/AVC Standard,’’ *48th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 07)/NEWCAS,* Montreal, Canada, Aug. 5-8, 2007.
- Abhijit Sil, Soumik Ghosh, and M.A. Bayoumi, ‘‘A Novel 8T SRAM Cell with Improved Read-SNM,’’ *48th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 07)/NEWCAS,* Montreal, Canada, Aug. 5-8, 2007.
- Zaher Merhi, Mohamed Elgamel, and M.A.Bayoumi, ‘‘Acoustic Target Localization in Wireless Sensor Network with FuzzyART,’’ *48th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 07)NEWCAS,* Montreal, Canada, Aug. 5-8, 2007.
- Zaher Merhi, Mohamed Elgamel, and M.A. Bayoumi, ‘‘Fully Decentralized Weighted Kalman Filter for Wireless Sensor Networks with FuzzyART Neural Networks,’’ *12th IEEE Symposium on Computers and Communications (ISCC 07),* Portugal, pp. 643-648, July 1-4, 2007.
- Abdelhamid Moursy, Ikhlas Ajbar, Dmitri Perkins and M.A. Bayoumi, ‘‘Building Empirical Models of Mobile Ad Hoc Networks,’’ *International Symposium on Performance Evaluation of Computer and Telecommunication Systems-SPECTS 2007,* San Diego, CA, July 2007.

- A. Abdelgawad and M.A. Bayoumi, ‘‘High Speed and Area-Efficient Multiply Accumulate (MAC) Unit for Digital Signal Processing Applications,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 07),* New Orleans, 27-30, 2007.
- Ruth Aguilar-Ponce, Jose-Luis Tecpanectl-Xihuitl, Ashok Kumar, and M.A. Bayoumi, ‘‘Pixel-Level Image Fusion Scheme based on Linear Algebra,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 07),* New Orleans, 27-30, 2007.
- Yasser Ismail, M. Shaaban, and M.A. Bayoumi, ‘‘An Adaptive Block Size Phase Correlation Motion Estimation Using Adaptive Early Search Termination Technique,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 07),* New Orleans, pp. 3423-3426, May 27-30, 2007.
- Xiaodong Zhang and M.A. Bayoumi, ‘‘A Low Power 4-bit Interleaved Burst Sampling ADC for Sub-GHz Impulse UWB Radio,’’ *IEEE International Symposium on Circuits And Systems (ISCAS 07),* New Orleans, pp. 1165-1168, May 27-30, 2007.
- Peiyi Zhao, Jason McNeely, M.A. Bayoumi, Pradeep Golconda, Kuang Weidong, ‘‘A Low Power Domino with Differential-Controlled-Keeper,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 07),* New Orleans, LA, pp. 1625-1628, May 27-30, 2007.
- Abhijit Sil, Soumik Ghosh, M.A. Bayoumi, ‘‘A Novel 90nm 8T SRAM With Enhanced Stability,’’ *IEEE International Conference on IC Design & Technology,* pp. 1661-1664, Austin, May 2007.
- Akl Charbel and M.A. Bayoumi, ‘‘Reducing Delay Uncertainty of On-Chip Interconnects by Combining Inverting and non-Inverting Repeaters Insertion,’’ *International Symposium on Quality Electronic Design(ISQED’07),* San Jose, California, March 2007.
- Akl Charbel and M.A. Bayoumi, ‘‘Transition Skew Coding: A Power and Area Efficient Encoding Technique for Global On-Chip Interconnects,’’ *Asia South Pacific Design Automation Conference (ASPDAC’07),* Yokohama, Japan, Jan. 2007, pp. 696-701.

2006

- Nan Wang, Azeez Sanusi and M.A. Bayoumi, ‘‘CTCNOC: A Central Caching Network-on-chip Communication Architecture Design,’’ *Proc. IP/SOC-2006 Conference,* Grenoble, France, December 6-7, 2006.
- Ruth Aguilar-Ponce, Jason McNeely, Abu Baker, Ashok Kumar, M.A. Bayoumi, ‘‘Multisensor Data Fusion Schemes for Wireless Sensor Networks,’’ *International Workshop on Computer Architecture for Machine Perception and Sensing,* Montreal, Canada, Sept. 2006.
- S. Goel, and M.A. Bayoumi, ‘‘Multi-path Search Algorithm for Block-based Motion Estimation,’’ to appear in *Proc. of the IEEE International Conference on Image Processing,* Atlanta, Oct. 2006.
- S. Goel, Y. Ismail, P. Devulapalli, J. McNeely, and M.A. Bayoumi, ‘‘An Efficient Data Re-use Motion Estimation Engine,’’ to appear in *Proceedings of the IEEE Workshop on Signal Processing Systems (SIPS 2005),* Banff, Canada, Sept. 2006.
- Zaher Merhi, Milad Ghantous, Mohammad Elgamel, M.A. Bayoumi, and Ayman El-Desouki, ‘‘A Fully-Pipelined Parallel Architecture for Kalman Tracking Filter,’’ *International Workshop on Computer Architectures for Machine Perception and Sensing (CAMP2006), Montreal, Canada, Sept. 18-21, 2006.*

- Xiaodong Zhang and M.A. Bayoumi, ‘‘A Low Power Adaptive Transmitter Architecture for Low Band UWB Applications,’’ *Proceedings of 2006 IEEE International Symposium on Circuit And Systems (ISCAS2006),* pp. 4727-4730, 2006.
- Ruth Aguilar-Ponce, Jose-Luis Tecpanectl-Xihuitl, Ashok Kumar, and M.A. Bayoumi, ‘‘Data Fusion Scheme for Tenet Architecture,’’ *IEEE International Workshop on Computer Architecture for Machine Perception and Sensing,* Montreal, Canada, Sept. 1820, 2006.
- Md Ibrahim Faisal, "M.A. Bayoumi," and Peiyi Zhao, ‘‘A Low-power Clock Frequency Multiplier,’’ *Proceedings of 2006 IEEE International Symposium on Circuits and Systems (ISCAS 2006),* pp. 1495-1498, May 2006.
- Mitun Bhattacharyya, Ashok Kumar, M.A. Bayoumi, ‘‘Design and Analysis of Energy Reference Metric in a Cluster Based Wireless Sensor Network,’’ *IEEE International Conference on Circuits and Systems for Communications (ICCSC 06),* Bucharest, Romania 6-7 July 2006.
- Mitun Bhattacharyya, Ashok Kumar, M.A. Bayoumi, ‘‘Algorithms for Energy-Efficient Query-Reduction in Wireless Sensor Networks,’’ *The International Workshop on Computer Architecture for Machine Perception and Sensing, (CAMPS 06),* Sept. 2006.
- Abu Baker, Soumik Ghosh, Ashok Kumar, M.A. Bayoumi, ‘‘ and Realization of Analog Phi-Function for LDPC Decoder,’’ *IEEE International Symposium on Circuits and Systems,* New Orleans, Louisiana, May 2007.
- Peiyi Zhao, Jason McNeely, Pradeep Golconda, M.A. Bayoumi, Kuang Weidong, ‘‘A Low Power High Fan in Differential Controlled Keeper Domino Design,’’ accepted for publication in *Proceedings of the International Symposium on Circuits and Systems (ISCAS),* May 27-30, 2007.
- Xiaodong Zhang and M.A. Bayoumi, ‘‘A Low Power 4-bit Interleaved Burst Sampling ADC for Sub-GHz Impulse UWB Radio,’’ accepted for *2007 IEEE International Symposium on Circuits and Systems (ISCAS2007),* May 2007.
- Ruth Aguilar-Ponce, Jose-Luis Tecpanectl-Xihuitl, Ashok Kumar, and M.A. Bayoumi, ‘‘Pixel-Level Image Fusion Scheme based on Linear Algebra,’’ to appear in *IEEE International Symposium on Circuits and Systems,* New Orleans, May 2007.
- Akl Charbel and M.A. Bayoumi, ‘‘Transition Skew Coding: A Power and Area Efficient Encoding Technique for Global On-Chip Interconnects,’’ *Asia South Pacific Design Automation Conference (ASPDAC’07),* Yokohama, Japan, Jan. 2007, pp. 696-701.
- Akl Charbel and M.A. Bayoumi, ‘‘Reducing Delay Uncertainty of On-Chip Interconnects by Combining Inverting and non-Inverting Repeaters Insertion,’’ to appear *International Symposium on Quality Electronic Design(ISQED’07),* San Jose, California, March 2007.
- Yasser Ismail, Mohsen Shaaban, and M.A. Bayoumi, ‘‘An Adaptive Block Size Phase Correlation Motion Estimation Using Adaptive Early Search Termination Technique,’’ accepted, *IEEE International Symposium on Circuits and Systems,* New Orleans, May 2007.

2005

- R. Aguilar-Ponce, J. Tessier, A. Baker, J. Das, C. Emmela, J.-L. Tecpanecatl-Xihuitl, A. Kumar, and M.A. Bayoumi, ‘‘VLSI Implementation of Wronskian Change Detector,’’ *IEEE Workshop on Signal Processing Systems (SiPS 2005),* 2-4 Nov. 2005, Athens, Greece.
- M. Elassal, A. Baker, and M.A. Bayoumi, ‘‘A Low Power VLSI Design Paradigm for Iterative Decoders,’’ *IEEE Signal Processing Systems,* 2-4 Nov. 2005, Athens, Greece.

- R.E. Aly, Md I. Faisal, and M.A. Bayoumi, ‘‘Novel 7T SRAM Cell for Low Power Cache Design,’’ *IEEE International ASIC/SOC Conference,* Sept. 2005, Jersey City, NJ.
- N. Wang and M.A. Bayoumi, ‘‘Dynamic Fraction Control Bus: New SOC On-chip Communication Architecture Design,’’ *IEEE International SOCC Conference (SOCC 05),* 25-28 Sept. 2005, Washington DC.
- R. Aguilar-Ponce, J. Tessier, A. Baker, J. Das, C. Emmela, J.-L. Tecpanecatl-Xihuitl, A. Kumar, and M.A. Bayoumi, ‘‘Real-Time VLSI Architecture for Detection of Moving Objects Using Wronskian Determinant,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),* 7-10 Aug. 2005, Cincinnati, OH.
- S. Goel, Y. Ismail and "M.A. Bayoumi," ‘‘Adaptive Search Window Size Algorithm for Fast Motion Estimation in H.264/AVC Standard,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),* 7-10 Aug. 2005, Cincinnati, OH.
- M. Kamal, M.A. Bayoumi, and A. Kumar, ‘‘An Efficient Polynomial-Modulus Based Technique for Multiplication of Large Integers,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),* 7-10 Aug. 2005, Cincinnati, OH.
- W. Elgharbawy, P. Golconda, A. Kumar, M.A. Bayoumi, ‘‘On Gate Leakage Reduction in Dynamic CMOS Circuits,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),* 7-10 Aug. 2005, Cincinnati, OH.
- A. Kumar, S. Goel, and M.A. Bayoumi, ‘‘A Fast Heuristic for Leakage-Aware Synthesis,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),* 7-10 Aug. 2005, Cincinnati, OH.
- J.-L. Tecpanectl-Xihuitl, R. Aguilar-Ponce, A. Kumar, and M.A. Bayoumi, ‘‘Design of a Power-Efficient Interleaved CIC Architecture for Software Defined Radio Receivers,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),* 7-10 Aug. 2005, Cincinnati, OH.
- X. Zhang, S. Ghosh and M.A. Bayoumi, ‘‘A Low Power CMOS UWB Pulse Generator,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),* 7-10 Aug. 2005, Cincinnati, OH.
- P. Zhao, G. Pradeep, J. McNeely, and M.A. Bayoumi, ‘‘External-Internal Dual Switch Leakage Controlled Flip-Flop Design,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005),* 7-10 Aug. 2005, Cincinnati, OH.
- R. Aguilar-Ponce, A. Kumar, J.-L. Tecpanectl-Xihuitl, and M.A. Bayoumi, ‘‘An Architecture for Automated Scene Understanding,’’ *IEEE International Workshop on Computer Architecture for Machine Perception (CAMP),* 4-6 July 2005, Terrasini - Palermo, Italy.
- N. Wang and M.A. Bayoumi, ‘‘A New SoC On-chip Communication Architecture Design,’’ *ESA 05*, 24-28 June 2005, Las Vegas, Nevada.
- S. Ghosh and M.A. Bayoumi, ‘‘On Integrated CMOS-MEMS Systems-on-Chip,’’ *IEEE International Northeast Workshop on Circuits and Systems (NEWCAS 2005),* pp. 31-34, 19-22 June 2005, Quebec City, Canada.
- R. Aly, M.A. Bayoumi, and M. Elgamel, ‘‘Dual Sense Amplified Bit Lines (DSABL) Architecture for Low-Power SRAM Design,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005),* 23-26 May 2005, Kobe, Japan.
- A. Chidanandan and M.A. Bayoumi, ‘‘Novel Systolic Array Architecture for the Decorrelator Using Conjugate Gradient for Least Squares Algorithm,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005),* pp. 5437-5440, 23-26 May 2005, Kobe, Japan.

- M. Elassal, A. Kumar, and M.A. Bayoumi, ‘‘A Systematic Framework for High Throughput MAP Decoder VLSI Architectures,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, pp. 29-32, 23-26 May 2005, Kobe, Japan.
- •. W. Elgharbawy, P. Golconda, A. Kumar, and M.A. Bayoumi, ‘‘A New Gate-level Body Biasing Technique for PMOS Transistors in Subthreshold CMOS Circuits,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, pp. 4697-4700, 23-26 May 2005, Kobe, Japan.
- Y. Li, M. Elgamel, M.A. Bayoumi, ‘‘A Partial Parallel Algorithm and Architecture for Arithmetic Encoder in JPEG2000,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, pp. 5198-5201, 23-26 May 2005, Kobe, Japan.
- J.L. Tecpanecatl-Xihuitl, A. Kumar, and M.A. Bayoumi, ‘‘Low Complexity Decimation Filter for Multi-standard Digital Receivers,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, 23-26 May 2005, Kobe, Japan.
- S. Ghosh, S. Venigalla, and M.A. Bayoumi, ‘‘Design and Implementation of a 2D-DCT Architecture using Coefficient Distributed Arithmetic Implementation Read Implementation,’’ *IEEE Computer Society Symposium on VLSI (ISVLSI 2005)*, pp. 162-166, 11-12 May 2005, Tampa, FL.
- Y. Li and M.A. Bayoumi, ‘‘Three-Level Parallel High Speed Architecture for EBCOT in JPEG2000,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2005)*, vol. 5, pp. 5-8, March 2005, Philadelphia, PA. Kobe, Japan.
- M. Elassal, A. Kumar, and M.A. Bayoumi, ‘‘A Systematic Framework for High Throughput MAP Decoder VLSI Architectures,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, pp. 29-32, 23-26 May 2005, Kobe, Japan.
- •. W. Elgharbawy, P. Golconda, A. Kumar, and M.A. Bayoumi, ‘‘A New Gate-level Body Biasing Technique for PMOS Transistors in Subthreshold CMOS Circuits,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, pp. 4697-4700, 23-26 May 2005, Kobe, Japan.
- Y. Li, M. Elgamel, M.A. Bayoumi, ‘‘A Partial Parallel Algorithm and Architecture for Arithmetic Encoder in JPEG2000,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, pp. 5198-5201, 23-26 May 2005, Kobe, Japan.
- J.L. Tecpanecatl-Xihuitl, A. Kumar, and M.A. Bayoumi, ‘‘Low Complexity Decimation Filter for Multi-standard Digital Receivers,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, 23-26 May 2005, Kobe, Japan.
- S. Ghosh, S. Venigalla, and M.A. Bayoumi, ‘‘Design and Implementation of a 2D-DCT Architecture using Coefficient Distributed Arithmetic Implementation Read Implementation,’’ *IEEE Computer Society Symposium on VLSI (ISVLSI 2005)*, pp. 162-166, 11-12 May 2005, Tampa, FL.
- Y. Li and M.A. Bayoumi, ‘‘Three-Level Parallel High Speed Architecture for EBCOT in JPEG2000,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2005)*, vol. 5, pp. 5-8, March 2005, Philadelphia, PA.

2004

- R.A. Ayoubi, H.A. Ziade, and M.A. Bayoumi, "An Efficient and Fault Tolerant Algorithm for Multilayer Neural Network," Intelligent Engineering Systems through Artificial Neural Networks, (ANNIE 2004), Eds: C.H. Dagli, et al., vol. 14, pp. 57-62.

- A. Chidanandan and M.A. Bayoumi, "Enhanced Parallel Interference Cancellation Using Decorrelator for the Base-Station Receiver," *IEEE International Symposium on Circuits and Systems (ISCAS 2004),* 23-26 May 2004, Vancouver, B.C., Canada.
- W. Elgharbawy, and M.A. Bayoumi, "B-DTNMOS: A Novel Bulk Dynamic Threshold NMOS Scheme," *IEEE International Symposium on Circuits and Systems (ISCAS 2004),* 23-26 May 2004, Vancouver, B.C., Canada.
- P. Zhao, G. P. Kumar and M.A. Bayoumi, "Contention Reduced/Conditional Discharge Flip-Flops for Level Conversion in CVS Systems," *IEEE International Symposium on Circuits and Systems (ISCAS 2004),* 23-26 May 2004, Vancouver, B.C., Canada.
- A. Fayed, W. Elgharbawy, and M.A. Bayoumi, "A Data Merging Technique for High-Speed Low-Power Multiply Accumulate Units," *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2004),* 18-21 May 2004, Montreal, Canada.
- P. Zhao, G. P. Kumar, A. Chidanandan and M.A. Bayoumi, "A Double-Edge Implicit-Pulsed Level Convert Flip-Flop," *IEEE Computer Society Symposium on VLSI (ISVLSI 2004),* pp. 141-144, 19-20 Feb. 2004, Lafayette, LA.

2003

- R.E. Aly, B.R. Nallamilli, and M.A. Bayoumi, "Variable-way Set-associative Cache Design for Embedded System Applications," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2003),* 27-30 Dec. 2003, Cairo, Egypt.
- M.A. Elgamel, S. Crochet, and M.A. Bayoumi, "Re-Spacing Framework for Interconnect Cross coupling Noise Reduction," *46th IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS 2003),* 27-30 Dec. 2003, Cairo, Egypt.
- W. Elgharbawy, and M.A. Bayoumi, "A Novel Ultra-Low-energy Bulk Dynamic Threshold PMOS Scheme," *IEEE International Midwest Symposium on Circuit and Systems (MWSCAS 2003),* 27-30 Dec. 2003, Cairo, Egypt.
- M.A. Elgamel, and M.A. Bayoumi, "An Efficient Minimum Area Spacing Algorithm for Noise Reduction," *10th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2003),* vol. 2, pp. 862-865, 14-17 Dec. 2003, Sharjah, UAE.
- Y. Li, H. Wu, D. Perkins, N.-F. Tzeng and M.A. Bayoumi, ‘‘MAC-SCC: Medium Access Control with a Separate control Channel for Multihop Wireless Networks,’’ *23rd International Conference on Distributed Computing Systems Workshops*, pp. 764-769, 2003.
- R.A. Ayoubi, H.A. Ziade, and M.A. Bayoumi, ‘‘Fault Tolerant Hopfield Associative Memory on Torus,’’ *18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 369-376, 3-4 Nov. 2003.
- M.K. Kourouma and M.A. Bayoumi, "Techniques for Increasing Capacity in Personal Area Networks," *WNCG Wireless Networking Symposium*, Oct. 2003.
- M.A. Elgamel and M.A. Bayoumi, "An Efficient Approach for Reducing Inductive Noise Using Shield Insertion [IC Layout]," *IEEE International SOC Conference*, pp. 203-206, 17-20 Sept. 2003, Portland, OR.
- M.A. Elgamel and M.A. Bayoumi, "Minimum-Area Shield Insertion for Explicit Inductive Noise Reduction," *16th Symposium on Integrated Circuits and Systems Design (SBCCI 2003),* pp. 256-260, 8-11 Sept. 2003, São Paulo, Brazil.
- S. Goel, M.A. Elgamel, and M.A. Bayoumi, "Novel Design Methodology for High-performance XOR-XNOR Circuit Design," *Proceedings 16th Symposium on Integrated*

Circuits and Systems Design (SBCCI 2003), pp. 71-76, 8-11 Sept. 2003, São Paulo, Brazil.

- T. Darwish and M.A. Bayoumi, "Energy Aware Distributed Arithmetic DCT Architectures," *IEEE Workshop on Signal Processing Systems (SiPS 2003),* pp. 351-356, 27-29 Aug. 2003, Seoul, South Korea.
- M. Elassal and M.A. Bayoumi, "A Low Power Turbo Decoder Architecture," *IEEE Workshop on Signal Processing Systems (SiPS 2003),* pp. 105-110, 27-29 Aug. 2003, Seoul, South Korea.
- A. Utgikar, W. Badawy, G. Seetharaman, and M.A. Bayoumi, "Affine Schemes in Mesh-based Video Motion Compensation," *IEEE Workshop on Signal Processing Systems (SiPS 2003),* pp. 159-164, 27-29 Aug. 2003, Seoul, South Korea.
- J.L. Tecpanecatl-Xihuitl and M.A. Bayoumi, "Efficient Multistage Decimation Filter Using Pipeline/Interleaving Architectures for Digital IF Receiver," *International Symposium on Signals, Circuits and Systems (SCS 2003),* pp. 25-28, 10-11 July 2003, Iasi, Romania.
- S. Goel, M. Shaaban, T. Darwish, H. Mahmoud, and M.A. Bayoumi, "Memory Accesses Reduction for MIME Algorithm," *International Conference on Multimedia and Expo ICME,* vol. 2, pp. 805-808, 6-9 July 2003.
- J.L. Tecpanecatl-Xihuitl, R.M. Aguilar-Ponce, M.A. Bayoumi, and B. Zavidovique, "Digital IF Decimation Filters for 3G Systems Using Pipeline/Interleaving Architecture," *Seventh International Symposium on Signal Processing and Its Applications,* vol. 2, pp. 327-330, 1-4 July 2003, Paris, France.
- S. Goel, M.A. Elgamel, and M.A. Bayoumi, "Energy Efficient and Noise-Tolerant XOR-XNOR Circuit Design," *The 2003 International Conference on VLSI (VLSI 03),* 23-26 June 2003, Las Vegas, NV.
- P. Zhao, T. Darwish, M.A. Bayoumi, "Low Power Conditional-Discharge Pulsed Flip-flops," *International Conference on Embedded Systems and Applications 2003,* pp. 204-209, 23-26 June 2003, Las Vegas, NV.
- M.K. Kourouma and M.A. Bayoumi, ‘‘Improving Capacity in Bluetooth Ad-hoc Networks,’’ *7th International Conference on Telecommunications (ConTEL 2003),* pp. 129-136, 11-13 June 2003.
- M.A. Elgamel, K.S. Tharmalingam, and M.A. Bayoumi, "Noise-Constrained Interconnect Optimization for Nanometer Technologies," *IEEE International Symposium on Circuits and Systems (ISCAS 2003),* vol. 5, pp. 481-484, 25-28 May 2003, Bangkok, Thailand.
- M.A. Elgamel, S. Goel, and M.A. Bayoumi, "Noise Tolerant Low Voltage XOR-XNOR for Fast Arithmetic," *2003 Great Lakes Symposium on VLSI (GLSVLSI 2003),* 28-29 April 2003, Washington D.C.
- Y. Li, R.E. Aly, M.A. Bayoumi, and S.A. Mashali, "Parallel High-Speed Architecture for EBCOT in JPEG2000," *International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2003),* vol. 2, pp. 481-484, 6-10 April 2003, Hong Kong.
- M.A. Elgamel, K.S. Tharmalingam, and M.A. Bayoumi, "Crosstalk Noise Analysis in Ultra Deep Submicrometer Technologies," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2003),* pp. 189-192, 20-21 Feb. 2003, Tampa, FL.
- S. Goel, T. Darwish, and M.A. Bayoumi, "A Novel Technique for Noise-tolerance in Dynamic Circuits," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI 1003),* pp. 203-206, 20-21 Feb. 2003.

- R.E. Aly, M.A. Bayoumi, and B. Zavidovique, ‘‘Novel Low Power and High-Speed Architecture for EBCOT Block in JPEG 2000,’’ *IEEE Asilomer Conference on Signal, Systems, and Computers* 2003, California.

2002

- T. Darwish and M.A. Bayoumi, ‘‘Reducing the Switching Activity of Modified SAFF Flip-Flop for Low Power Applications,’’ *The 14th International Conference on Microelectronics (ICM 2002)*, pp. 96-99, 11-13 Dec. 2002, Beirut Lebanon.
- M.A. Elgamel, B.R. Nallamilli, and M.A. Bayoumi, ‘‘Systolic Array Architectures for Full-Search Block Matching Motion Estimation,’’ *Third International Workshop on Digital and Computational Video (DCV 2002)*, pp. 108-115, 14-15 Nov. 2002, Clearwater Beach, FL.
- H. Mahmoud, S. Goel, M. Shaaban, T. Darwish, and M.A. Bayoum, ‘‘A Low Power VLSI Architecture for Multistage Interval-based Motion Estimation (MIME) Algorithm,’’ *Third International Workshop on Digital and Computational Video (DCV 2002)*, pp. 159-166, 14-15 Nov. 2002.
- S.K. Sadhu, M.A. Elgamel, and M. A. Bayoumi, ‘‘Low Power Full Search Block Matching Motion Estimation Architecture,’’ *Third International Workshop on Digital and Computational Video (DCV 2002)*, pp. 123-128, 14-15 Nov. 2002, Clearwater Beach, FL.
- M. El-Assal and M.A. Bayoumi, ‘‘A High Speed Architecture for Map Decoder,’’ *IEEE Workshop on Signal Processing Systems (SiPS 2002)*, pp. 69-74, 16-18 Oct. 2002.
- M.A. Elgamel and M.A. Bayoumi, ‘‘On Low Power High Level Synthesis Using Genetic Algorithms,’’ *9th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2002)*, vol. 2, pp. 725-728, 15-18 Sept. 2002, Dubrovnik, Croatia.
- T. Darwish and M.A. Bayoumi, ‘‘Ultra Low Power 1-Bit Adder Cells,’’ *IEEE International Midwest Symposium on Circuits And Systems (MWCAS 2002)*, vol. 2, pp. 290-293, 4-7 Aug. 2002, Tulsa OK.
- M. El-Assal and M.A. Bayoumi, ‘‘Map Decoder Architecture: Soft IP for SoC Applications,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2002)*, vol. 2, pp. 95-98, 4-7 Aug. 2002, Tulsa, OK.
- M.A. Elgamel, S. Crochet, and M.A. Bayoumi, ‘‘SOC Interconnect in Deep Submicron,’’ *IIEEE International Midwest Symposium on Circuits and Systems, (MWSCAS 2002)*, vol. 2, pp. 103-106, 4-7 Aug. 2002, Tulsa, OK.
- Y. Li, R.E. Aly, B. Wilson, and M.A.Bayoumi, ‘‘Analysis and Enhancements for EBCOT in High-Speed JPEG2000 Architectures,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2002)*, vol. 2, pp. 207-210, 4-7 Aug. 2002, Tulsa, OK.
- K. Rawat, T. Darwish and M.A. Bayoumi, ‘‘A Low Power And Reduced Area Carry Select Adder,’’ *IEEE International Midwest Symposium on Circuits And Systems (MWCAS 2002)*, pp. 467-470, 4-7 Aug. 2002, Tulsa, OK.
- P. Zhao, T. Darwish and M.A. Bayoumi, ‘‘Low Power and High Speed Explicit-Pulsed Flip-Flops,’’ *IEEE International Midwest Symposium on Circuits And Systems (MWCAS 2002)*, vol. 2, pp. 477-480, 4-7 Aug. 2002, Tulsa, OK.
- R.A. Ayoubi and M.A. Bayoumi, ‘‘An Efficient Implementation of Multi-layer Perceptron on Mesh Architecture,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2002)*, vol. 2, pp. 109-112, 26-29 May 2002.

- M. El-Assal and M.A. Bayoumi, ‘‘Low Power SOVA Architecture Using Bi-directional Scheme,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2002)*, vol. 1, pp. 277-280, 26-29 May 2002.
- A.A. Fayed and M.A. Bayoumi, ‘‘Noise-Tolerant Design and Analysis for a Low-voltage Dynamic Full Adder Cell,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2002)*, vol. 2, pp. 579-582, 26-29 May 2002.
- A.A. Fayed and M.A. Bayoumi, ‘‘A Merged Multiplier-accumulator for High Speed Signal Processing Applications,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2002)*, vol. 3, pp. 3212-3215, 13-17 May 2002.
- M. Elgamel, T. Darwish and M.A. Bayoumi, ‘‘Noise Tolerant Low Power Dynamic TSPCL D Flip-Flops,’’ *IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2002)*, pp. 80-85, 25-26 April 2002, Pittsburgh, PA.
- A. Shams, W. Pan, A. Chidanandan, and M.A. Bayoumi, ‘‘A Low Power Performance Distributed DCT Architecture,’’ *IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2002)*, pp. 21-27, 25-26 April 2002.

2001

- M.K. Kourouma and M.A. Bayoumi, "Voice Over Wireless ATM Networks," *6th International Conference on Telecommunications (ConTEL 2001)*, pp. 79-83, 13-15 June 2001, Zagreb, Croatia.
- W. Badawy and M.A. Bayoumi, ‘‘A Mesh Based Motion Tracking Architecture,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2001)*, vol. 4, pp. 262-265, 6-9 May 2001, Sydney, Australia.
- M.A. Elgamel, A. Shams, X. Xueling, and M.A. Bayoumi, ‘‘Enhanced Low Power Motion Estimation VLSI Architectures for Video Compression,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2001)*, vol. 4, pp. 474-477, 6-9 May 2001, Sydney, Australia.
- A. Fayed and M.A. Bayoumi, ‘‘A Low Power 10 Transistor Full Adder Cell for Embedded Architectures,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2001)*, vol. pp. 226-229, 6-9 May 2001, Sydney, Australia.
- A. Fayed and M.A. Bayoumi, ‘‘A Novel Architecture for Low-Power Design of Parallel Multipliers,’’ *IEEE Computer Society Annual Workshop on VLSI (WVLSI 2001)*, pp. 149-154, 19-20 April 2001, Orlando, FL.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘An Efficient Low Bit Rate Adaptive Mesh Based Motion Compensation Technique,’’ *Second USF International Workshop on Digital and Computational Video (DCV 2001)*, pp. 164-172, 8-9 Feb. 2001, Tampa, FL.
- A.M. Shams, M.A. Elgamel, and M.A. Bayoumi, ‘‘Hybrid Mesh-Based/Block-Based Motion Compensation Architecture,’’ *Second USF International Workshop on Digital and Computational Video (DCV 2001)*, pp. 194-201, 8-9 Feb. 2001, Tampa, FL.

2000

- W. Badawy and M.A. Bayoumi, ‘‘A Scalable Affine Core for Mesh-based Video Object Motion Compensation,’’ *7th IEEE International Conference on Electronics, Circuits & Systems (ICECS 2000)*, vol. 2, pp. 663-666, 17-20 Dec. 2000, Kaslik, Lebanon.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘An Efficient Low-bit Rate Adaptive Mesh-based Motion Compensation Technique,’’ *7th IEEE International Conference on Electronics, Circuits & Systems (ICECS 2000)*, pp. 491-494, 17-20 Dec. 2000, Kaslik, Lebanon.

- T. Darwish, A. Vyas, W. Badawy, and M.A. Bayoumi, ‘‘A Low Power VLSI Prototype for Low Bit Rate Video Applications,’’ *IEEE Workshop on Signal Processing Systems (SiPS 2000)*, pp. 159-167, 11-13 Oct. 2000, Lafayette, LA.
- M.A. Elgamel, A. Shams, and M.A. Bayoumi, ‘‘A Comparative Analysis for Low Power Motion Estimation VLSI Architectures,’’ *IEEE Workshop on Signal Processing Systems (SiPS 2000)*, pp. 149-158, 11-13 Oct. 2000, Lafayette, LA.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘An Efficient Low Bit-Rate Adaptive Mesh-based Motion Compensation Technique,’’ *IEEE Workshop on Signal Processing Systems (SiPS 2000)*, pp. 139-148, 11-13 Oct. 2000, Lafayette, LA.
- B. Wilson, et al., ‘‘A Memory Efficient Architecture for Compressed-Domain Texture Feature Extraction,’’ *IEEE Workshop on Signal Processing Systems (SiPS 2000)*, pp. 305-314, 11-13 Oct. 2000, Lafayette, LA.
- W. Badawy and M.A. Bayoumi, ‘‘Low Power Video Object Motion-tracking Architecture for Very Low Bit Rate Online Video Applications,’’ *International Conference on Computer Design (ICCD 2000)*, pp. 533-536, 17-20 Sept. 2000, Austin, TX.
- W. Badawy and M.A. Bayoumi, ‘‘Low Power VLSI Prototype for Motion Tracking Architecture,’’ *13th Annual IEEE International ASIC/SOC Conference*, pp. 243-247, 13-16 Sept. 2000, Washington, D.C.
- W. Badawy and M.A. Bayoumi, ‘‘Scalable Affine Core for Video Object Motion Compensation,’’ *International Workshop on Computer Architectures for Machine Perception (CAMP 2000)*, pp. 142-146, 11-13 Sept. 2000, Padova, Italy.
- B. Wilson and M.A. Bayoumi, ‘‘Compressed-Domain Classification of Texture Images,’’ *International Workshop on Computer Architectures for Machine Perception (CAMP 2000)*, pp. 347-355, 11-13 Sept. 2000, Padova, Italy.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘A New Block-Matching Motion Estimation Algorithm Based on Successive Elimination,’’ *IEEE International Conference on Image Processing (ICIP 2000)*, vol. 3, pp. 608-611, 10-13 Sept. 2000, Vancouver, BC, Canada.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘A Low Power Architecture for a New Efficient Block-Matching Motion Estimation Algorithm,’’ *43rd Midwest Symposium on Circuits and Systems (MWSCAS 2000)*, pp. 436-439, 8-11 Aug. 2000, Lansing, MI.
- B. Wilson and M.A. Bayoumi, ‘‘An EZW Compressed Image Technique for Calculating Texture Signatures,’’ *43rd Midwest Symposium on Circuits and Systems (MWSCAS 2000)*, vol. 2, pp. 600-603, 8-11 Aug. 2000, Lansing, Michigan.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘An Efficient Low-Bit Rate Motion Compensation Technique Based on Quadtree,’’ *International Conference on Multimedia and Expo 2000 (ICME 2000)*, pp. 213-216, 30 July-2 Aug. 2000, New York, NY.
- W. Badawy and M.A. Bayoumi, ‘‘A Multiplication-Free Parallel Architecture for Affine Transformation,’’ *IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP 2000)*, pp. 25-34, 10-12 July 2000, Boston, MA.
- A. Shams and M.A. Bayoumi, ‘‘A 108Gbps, 1.5GHz 1D-DCT Architecture,’’ *IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP 2000)*, pp. 163-172, 10-12 July 2000, Boston, MA.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘Low Bit-Rate Generalized Quadtree Motion Compensation Algorithm and its Optimal Encoding Scheme,’’ *SPIE’s Visual Communications and Image Processing 2000*, 20-23 June 2000, Perth, Australia.

- W. Badawy and M.A. Bayoumi, ‘‘A VLSI Architecture for 2D Mesh-based Video Object Motion Estimation,’’ *International Conference on Consumer Electronics 2000*, pp. 124-125, 13-15 June 2000, Los Angeles, CA.
- W. Badawy and M.A. Bayoumi, ‘‘On Minimizing Hierarchical Mesh Coding Overhead: (HASM) Hierarchical Adaptive Structured Mesh Approach,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2000)*, vol. 4, pp. 1923-1926, 5-9 June 2000, Istanbul, Turkey.
- W. Badawy, et al., ‘‘A VLSI Architecture for Hierarchical Mesh-based Motion Compensation Using Scalable Affine Transformation Core,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2000)*, pp. 659-663, 28-31 May 2000, Geneva, Switzerland.
- A. Shams, W. Pan, A. Chandanandan and M.A. Bayoumi, ‘‘A High-Performance Architecture for the 1D-DCT,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 2000)*, vol. 5, pp. 521-524, 28-31 May 2000, Geneva, Switzerland.
- W. Badawy and M.A. Bayoumi, ‘‘Low Power VLSI Architecture For 2D-Mesh Video Object Motion Tracking,’’ *IEEE Computer Society Annual Workshop on VLSI*, pp. 67-72, 27-28 April 2000, Orlando, FL.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘An Efficient Successive Elimination Algorithm for Block-matching Motion Estimation,’’ *Data Compression Conference (DCC 2000)*, pg. 559, 28-30 March 2000.
- H.A. Mahmoud and M.A. Bayoumi, ‘‘An Efficient Low-bit Motion Compensation Technique Based on Quadtree,’’ *Data Compression Conference (DCC 2000)*, pg. 560, 28-30 March 2000.
- B. Wilson and M.A. Bayoumi, ‘‘Compressed Domain Texture Classification from a Modified EZW Symbol Stream,’’ *Data Compression Conference (DCC 2000)*, pg. 527, 28-30 March 2000.
- W. Badawy and M.A. Bayoumi, ‘‘A VLSI Architecture for Hybrid Object-based Video Motion Estimation,’’ *IEEE Canadian Conference on Electrical and Computer Engineering*, vol. 2, pp. 1109-1113, 7-10 March 2000, Helifax, Nova Scotia.

1999

- W. Badawy, G. Zhang, M. Talley, M. Weeks and M.A. Bayoumi, ‘‘A Low Power 3-D Discrete Wavelet Transform Processor for Medical Application,’’ *IEEE Workshop on Signal Processing Systems (SiPS 1999)*, pp. 65-74, 20-22 Oct. 1999, Taipei, Taiwan.
- W.M. Badawy, G. Zhang, and M.A. Bayoumi, ‘‘VLSI Architecture for Hierarchical Mesh-based Motion Estimation,’’ *IEEE Workshop on Signal Processing Systems (SiPS 1999)*, pp. 110-119, 20-22 Oct. 1999, Taipei, Taiwan.
- W.M. Badawy, A. Kumar and M.A. Bayoumi, ‘‘A Co-design Based High-Performance Real-Time GIS,’’ *IEEE Workshop on Signal Processing Systems (SiPS 1999)*, pp. 410-419, 20-22 Oct. 1999, Taipei, Taiwan.
- W. Pan, A. Shams, M.A. Bayoumi, ‘‘NEDA: A New Distributed Arithmetic Architecture and its Application to One Dimensional Discrete Cosine Transform,’’ *IEEE Workshop on Signal Processing Systems (SiPS 1999)*, pp. 159-168, 20-22 Oct. 1999, Taipei, Taiwan.
- A. Kumar and M.A. Bayoumi, ‘‘Novel Formulations for Low-power Binding of Function Units in High-level Synthesis,’’ *International Conference on Computer Design (ICCD 1999)*, pp. 321-324, 10-13 Oct. 1999.

- M.M. Al-Khatib and M.A. Bayoumi, ‘‘Performance Analysis for a New Automatic Error Control System for Overcoming Atmospheric Multipath Fading with Random Bit Errors for Wireless ATM Networks,’’ *Wireless Communications and Networking Conference (WCNC 1999)*, vol. 3, pp. 1407-1411, 21-24 Sept. 1999.
- W. Badawy and M.A. Bayoumi, ‘‘A Low Power and High Performance Core for Planar Object Overlaying,’’ *IEEE International Conference on Electronics, Circuits and System (ICECS 1999)*, 5-8 Sept. 1999, Paphos, Cyprus.
- A. Kumar and M.A. Bayoumi, ‘‘Methodologies for Binding Function Units for Low Power in High Level Synthesis,’’ *6th IEEE International Conference on Electronics, Circuits and Systems (ICECS 1999)*, vol. 2, 907-910, 5-8 Sept. 1999.
- W. Badawy and M.A. Bayoumi, ‘‘A Low-Power Pipelined Map Overlaying Architecture for Hand Held Applications,’’ *European Conference on Circuit Theory and Design (ECCTD 1999)*, vol. 2, pp. 621-624, 29 Aug.-2 Sept. 1999, Stresa, Italy.
- W.M. Badawy, G. Zhang and M.A. Bayoumi, ‘‘A Low Power Prototype for a Motion Estimation Processor,’’ *42nd Midwest Symposium on Circuits and Systems (MWSCAS 1999)*, 8-11 Aug. 1999, Las Cruces, NM.
- W. Badawy, G. Zhang, and M.A. Bayoumi, ‘‘VLSI Architecture for Hierarchical 2D Mesh Representation for Very Low Bit Rate Applications, *42nd Midwest Symposium on Circuits and Systems (MWSCAS 1999)*, pp. 77-80, 8-11 Aug. 1999, Las Cruces, NM.
- A. Kumar and M.A. Bayoumi, ‘‘Low-power Binding of Function Units in High-level Synthesis,’’ *42nd Midwest Symposium on Circuits and Systems (MWSCAS 1999)*, pp. 214-217, 8-11 Aug. 1999, Las Cruces, NM.
- A. Shams and M.A. Bayoumi, ‘‘A Framework for Fair Performance Evaluation of 1-bit Full Adder Cells,’’ *42nd Midwest Symposium on Circuits and Systems (MWSCAS 1999)*, pp. 6-9, 8-11 Aug. 1999, Las Cruces, NM.
- M.M. Al-Khatib and M.A. Bayoumi, ‘‘Performance Analysis for a New Automatic Error Control System for Overcoming Turbulent Fading Errors for Wireless ATM Networks,’’ *IEEE International Symposium on Computers and Communications (ISCC 1999)*, pp. 310-316, 6-8 July 1999.
- M.M. Al-Khatib and M.A. Bayoumi, ‘‘New Error Control Enhancing Technique for Wireless ATM Networks,’’ *2nd International Conference on ATM (ICATM 1999)*, pp. 425-429, 21-23 June 1999.
- W.M. Badawy and M.A. Bayoumi, ‘‘A Low Cost Real Time Motion Estimation VLSI Core,’’ *International Workshop on Design, Test and Applications (WTAD 1999)*, 14-16 June 1999, Dubrovnik, Croatia.
- M.M. Al-Khatib and M.A. Bayoumi, Performance Analysis for a New Wireless ATM Automatic Control System," *WMATM 1999*, 2-4 June 1999, San Francisco, CA.
- A. Kumar and M.A. Bayoumi, ‘‘Multiple Voltage-based Scheduling Methodology for Low Power in the High Level Synthesis,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1999)*, pp. 371-374, 30 May-2 June 1999.
- A. Kumar, M.A. Bayoumi, and R. Cherabuddi, ‘‘Minimizing Switchings of the Function Units through Binding for Low Power,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1999)*, pp. 66-69, 30 May-2 June 1999.
- M.B. Maaz and M.A. Bayoumi, ‘‘A Non-zero Clock Skew Scheduling Algorithm for High peed Clock Distribution Network,’’ *IEEE International Symposium on Circuits and Systems*

(ISCAS 1999), vol. 6, pp. 382-385, 30 May-2 June 1999.

- H.A. Mahmoud and M.A. Bayoumi, ‘‘A 10-Transistor Low-Power High-Speed Full Adder Cell,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1999)*, pp. 43-46, 30 May-2 June 1999, Orlando, FL.
- A. Shams and M.A. Bayoumi, ‘‘Performance Evaluation of 1-bit CMOS Adder Cells,’’ *IEEE International Symposium on Circuits and Systems (ISCAS ’99)*, pp. 27-30, 30 May-2 June 1999, Orlando, FL.
- G. Zhang, M. Talley, W. Badawy, M. Weeks and M.A. Bayoumi, ‘‘A Low Power Prototype for a 3-D Discrete Wavelet Transform Processor,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1999)*, pp. 145-148, 30 May-2 June 1999, Orlando, FL.
- M.M. Al-Khatib and M.A. Bayoumi, ‘‘New Automatic Error Control System with ATM Cell Header Reduction for Wireless ATM Networks,’’ *IEEE Proceedings, ATM Workshop*, pp. 233-238, 24-27 May 1999.

1998

- A.M. Shams, W.M. Badawy, and M.A. Bayoumi, ‘‘An Enhanced Low-Power Computational Kernel for a Pipelined Multiplier-Accumulator Unit,’’ *Tenth International Conference on Microelectronics (ICM 1998)*, pp. 33-36, 14-16 Dec. 1998, Monastir, Tunisia.
- A. Kumar and M.A. Bayoumi, ‘‘A Novel Scheduling-based CAD Methodology for Exploring the Design Space for Low Power,’’ *IEEE Asia-Pacific Conference on Circuits and Systems*, pp. 391-394, 24-27 Nov. 1998.
- M. Weeks, J. Limqueco, and M.A. Bayoumi, ‘‘On Block Architectures for Discrete Wavelet Transform,’’ *32nd Asilomar Conference on Signals, Systems and Computers*, vol. 2, pp. 1022-1026, 1-4 Nov. 1998.
- W.M. Badawy, A.M. Shams, and M.A. Bayoumi, ‘‘An Enhanced Low-Power Pipelined Multiplier-Accumulator for DSP Applications,’’ *7th NASA Symposium on VLSI*, 1-2 Oct. 1998, Albuquerque, NM.
- A. Kumar and M.A. Bayoumi, ‘‘A Novel Scheduling-based CAD Methodology for Exploring the Design Space of ASICs for Low Power,’’ *11th Annual IEEE International ASIC Conference*, pp. 115-118, 13-16 Sept. 1998.
- H. Krishnamurthy, M.B. Maaz, and M.A. Bayoumi, ‘‘A New Partitioning Framework for Uniform Clock Distribution during High-Level Synthesis,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1998)*, vol. 6, pp. 381-384, 31 May-3 June 1998.
- A.M. Shams and M.A. Bayoumi, ‘‘A Novel Low-power Building Block CMOS Cell for Adders,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1998)*, vol. 2, pp. 153-156, 31 May-3 June 1998.
- M. Weeks and M.A. Bayoumi, ‘‘3-D Discrete Wavelet Transform Architectures,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1998)*, vol. 4, pp. 57-60, 31 May-3 June 1998.
- A.M. Shams and M.A. Bayoumi, ‘‘A New Full Adder Cell for Low-power Applications,’’ *8th Great Lakes Symposium on VLSI (GLS 1998)*, pp. 45-49, 19-21 Feb. 1998.

1997

- A. Shams and M.A. Bayoumi, ‘‘A Structured Approach for Designing Low Power Adders,’’ *31st IEEE Asilomer Conference on Signal, Systems, and Computers*, pp. 757-761, 2-5 Nov. 1997.

- S. Yazji, B. Lumetta, M.A. Bayoumi, and B. Zavidovique, ‘‘A Motion-Estimation Architecture Based on Band-Matching,’’ *Proc. 32nd IEEE Asilomer Conference on Circuits, Signals, and Computers*, pp. 421-425, 2-5 Nov. 1997.
- R.V. Cherabuddi and M.A. Bayoumi, ‘‘A Low Power Based Partitioning and Binding Technique for Single Chip Application Specific DSP Architectures,’’ *2nd IEEE International Conference on Innovative Systems in Silicon*, pp. 35-361, 8-10 Oct. 1997, Austin, TX.
- J.C. Limqueco and M.A. Bayoumi, ‘‘Block Computation Architectures for 2-D Discrete Wavelet Transforms,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1997)*, vol. 2, pp. 865-868, 3-6 Aug. 1997.
- A. Sayed and M.A. Bayoumi, ‘‘A New Low Power Building Block Cell for Adders,’’ *IEEE Midwest Symposium on Circuits and Systems (MWSCAS 1997)*, vol. 2, pp. 818-822, 3-6 Aug. 1997.
- S. Yazji, B. Lumetta, M.A. Bayoumi, and B. Zavidovique, ‘‘A Band-Matching Approach for Motion Estimation,’’ *IEEE Midwest Symposium on Circuits and Systems (MWSCAS 1997)*, vol. 2, pp. 909-912, 3-6 Aug. 1997.
- S. Yazji, M.A. Bayoumi, B. Zavidovique, ‘‘A Motion-Estimation Parallel Algorithm Based on Band-Matching,’’ *SPIE, Parallel and Distributed Methods for Image Processing*, pp. 241-263, July 1997.
- B.A. Alhalabi and M.A. Bayoumi, ‘‘On-Chip Learning for a Scalable Hybrid Neural Architecture,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1997)*, pp. 677-680, 9-12 June 1997, Hong Kong.
- D.F. Seidel and M.A. Bayoumi, ‘‘A Multicasting ATM Switch Architecture,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1997)*, pp. 2140-2143, 9-12 June 1997, Hong Kong.
- M. Al-Khatib, A. Kumar, S. Rajupalem and M.A. Bayoumi, ‘‘A New Architectural Design for a Deflecting Multicast Switch,’’ *4th International Conference on Telecommunications*, pp. 149-157, June 1997, Zagreb, Croatia.
- R.V. Cherabuddi, M.A. Bayoumi, H. Krishnamurthy, ‘‘A Low Power Based System Partitioning and Binding Technique for Multi-Chip Module Architectures,’’ *7th IEEE Great Lakes Symposium on VLSI (GLS 1997)*, pp. 156-162, 13-15 March 1997.
- M. Weeks, M.B. Maaz, H. Krishnamurthy, P. Shipley, and M.A. Bayoumi, ‘‘A Prototype Chipset for a Large Scalable ATM Switching Node,’’ *7th IEEE Great Lakes Symposium on VLSI (GLS 1997)*, pp. 131-136, 13-15 March 1997.

1996

- J. Limqueco and M.A. Bayoumi, A Scalable Architecture for 2D Discrete Wavelet Transform,’’ *IEEE VLSI Signal Processing Workshop*, pp. 369-377, 30 Oct.-1 Nov. 1996, San Francisco, CA.
- D. Seidel, A.R. Kaju, M.A. Bayoumi, ‘‘A New ATM Switch Architecture: Scalable Shared Buffer,’’ *3rd IEEE International Conference on Electronics, Circuits, and Systems (ICECS 1996)*, vol. 2, pp. 772-775, 13-16 Oct. 1996, Rodos, Greece.
- P. Shipley, M. Weeks, and M.A. Bayoumi, ‘‘A Scaleable Very Large ATM Switch Architecture for Bursting Traffic,’’ *International Conference on Computer and Communication Networks (ICCCN 1996)*, Sept. 1996, Washington, DC.

- P. Shipley, M. Weeks, and M.A. Bayoumi, ‘‘A Controller Chip for a Scaleable ATM Switch Node,’’ *Midwest Symposium on Circuits and Systems (MWSCAS 1996)*, pp. 73-76, 18-21 Aug. 1996.
- E. Abu-Shama, M. Maaz, and M.A. Bayoumi, ‘‘A Low-Power Fast Multiplier Architecture,’’ *Midwest Symposium on Circuits and Systems (MWSCAS 1996)*, 18-21 Aug. 1996.
- J.C. Limqueco and M.A. Bayoumi, ‘‘A High-Speed Array Architecture for 2-D Wavelet Transform,’’ *Midwest Symposium on Circuits and Systems (MWSCAS 1996)*, vol. 3, pp. 1239-1242, 18-21 Aug. 1996.
- B. Alhalabi and M.A. Bayoumi, ‘‘On-Chip Learning,’’ *4th IEEE Mediterranean Symposium on New Direction in Control and Automation*, pp. 770-775, June 1996, Greece.
- E. Abu-Shama and M.A. Bayoumi, et al., ‘‘Low Power Adders for DSP Architectures,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1996)*, May 1996, Atlanta.
- R. Ayoubi, A. Elchouemi, and M.A. Bayoumi, ‘‘An Efficient Mapping Algorithm of Multilayer Perception of Mesh-Connected Architectures,’’ *International Phoenix Conference on Computers and Communications*, pp. 188-193, 27-29 March 1996, Arizona.
- P. Shipley, S. Sayed and M.A. Bayoumi, ‘‘A High Speed VLSI Architecture for Scaleable ATM Switches,’’ *Sixth Great Lakes Symposium on VLSI (GLS 1996)*, pp. 72-76, 22-23 March 1996.
- R.V. Cherabuddi, J. Chen, and M.A. Bayoumi, ‘‘A Graph Based Approach to the Synthesis of Multi-chip Module Architectures,’’ *Ninth International Conference on VLSI Design*,’’ *pp. 192-197, 3-6 Jan. 1996.*

1995

- M. Altuwaijri and M.A. Bayoumi, ‘‘A New Recognition System for Multi-Font Arabic Cursive Words,’’ *2nd Annual International Conference on Electronics, Circuits, and Systems (ICECS 1995)*, Dec. 1995, Jordan.
- J. Chen and M.A. Bayoumi, ‘‘A Scalable Systolic Array Architecture for 2-D Discrete Wavelet Transforms,’’ *IEEE Workshop on VLSI Signal Processing VIII*, pp. 303-322, 16-18 Sept. 1995.
- S.B. Sayed and M.A. Bayoumi, ‘‘A Scalable Architecture for Discrete Wavelet Transform,’’ *Computer Architecture for Machine Perception (CAMP 1995)*, pp. 44-50, 18-20 Sept. 1995, Italy.
- P. Shipley and M.A. Bayoumi, ‘‘A Scalable Multibuffer ATM Switch Architecture,’’ *ISCA International Conference on Parallel and Distributed Computing Systems*, pp. 313-317, Sept. 1995.
- Q. Malluhi, R. Ayoubi, and M.A. Bayoumi, ‘‘The Associative SIMD Hypercube,’’ *ISCA International Conference on Parallel and Distributed Computing Systems*, pp. 458-464, Sept. 1995.
- A. Agrawal, M.A. Bayoumi, and A. Elchouemi, ‘‘A New ATM Congestion Control Scheme for Shared Buffer Switch Architectures,’’ *4th International Conference on Computer Communications and Networks*, pp. 604-611, Sept. 1995.
- E. Abu-Shama, A. Elchouemi, S. Sayed, and M.A. Bayoumi, ‘‘An Efficient Low Power Basic Cell for Adders,’’ *Midwest Symposium on Circuits and Systems (MWSCAS 1995)*, pp. 306-309, 13-16 Aug. 1995, Rio de Janeiro, Brazil.

- B. Alhalabi and M.A. Bayoumi, ‘‘A Scalable Hybrid Neural Accelerator,’’ *World Congress on Neural Networks 1995*, vol. 3, pp. 223-229, July 1995.
- M. Altuwaijri and M.A. Bayoumi, ‘‘A New Thinning Algorithm for Arabic Character using Self-Organizing Neural Network,’’ *IEEE International Symposium on Circuits and Systems (MWSCAS 1995)*, vol. 3, pp. 1824-1827, 28 April-3 May 1995.
- A. Sri-Krishna, C. Chu, and M.A. Bayoumi, ‘‘FFT Based Fast Architecture and Algorithm for Discrete Wavelet Transforms,’’ *Data Compression Conference (DCC 1995)*, pg. 441, 28-30 March 1995.
- B. Alhalabi and M.A. Bayoumi, ‘‘A Scalable Analog Architecture for Neural Networks with On-chip Learning and Refreshing,’’ *Great Lakes Symposium on VLSI (GLS 1995)*, pp. 33-38, 16-18 March 1995.
- A. Agrawal, A. Raju, S. Varadarajan, and M.A. Bayoumi, ‘‘A Scalable Shared Buffer ATM Switch Architecture,’’ *Great Lakes Symposium on VLSI (GLS 1995)*, pp. 256-261, 16-18 March 1995.
- N. Maldonado, G. Andrus, A. Tyagi, M. Madani, and M.A. Bayoumi, ‘‘A Post-processing Algorithm for Short-circuit Defect Sensitivity Reduction in VLSI Layouts,’’ *7th Annual IEEE International Conference on Wafer Scale Integration*, pp. 288-297, 18-20 Jan. 1995.

1994

- A. Agrawal, A. Raju, M.A. Bayoumi, ‘‘A Scalable Shared Multibuffer Switch Architecture for ATM,’’ *International Conference on Electronics, Circuits, and Systems (ICECS 1994)*, Dec. 1994.
- M. Altuwaijri and M.A. Bayoumi, ‘‘Recognition of Arabic Characters using Neural Networks,’’ *International Conference on Electronics, Circuits, and Systems (ICECS 1994)*, Dec. 1994.
- L.-Y. Chiou, J. Limqueco, M.A. Bayoumi, ‘‘A VLSI Architecture for Modified Frequency Sensitive Self-Organizing Neural Network for Image Data Compression,’’ *1994 IEEE Workshop on VLSI Signal Processing VII*, pp. 418-424, 26-28 Oct. 1994.
- Q. M. Malluhi, M.A. Bayoumi, T.R.N. Rao, ‘‘ANN Processing on SIMD Hypercubes,’’ *7th International Conference on Parallel and Distributed Systems*, Oct. 1994.
- D. Seidel, P. Shipley, and M.A. Bayoumi, ‘‘A Scalable Architecture for a Distributed ATM Switch,’’ *7th International Conference on Parallel and Distributed Systems*, Oct. 1994.
- B.A. Alhalabi, M.A. Bayoumi, and A.A. El-Amawy, ‘‘A Slice of a Brain: A Hybrid Neural Chip Set,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1994)*, pp. 489-494, 3-5 Aug. 1994.
- A. El-Amawy, P. Kulasinghe, and M.A. Bayoumi, ‘‘Optimal Mapping of Feedforward Neural Networks onto Multiple Bus Architectures, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1994)*, pp. 477-483, 3-5 Aug. 1994.
- Q.M. Malluhi, M.A. Bayoumi, and T.R.N. Rao, ‘‘Design of Digital Accelerators for Backpropagation,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1994)*, pp. 484-488, 3-5 Aug. 1994.
- P.E. Shipley, D.F. Seidel, and M.A. Bayoumi, ‘‘A Building Block Chip for a Scaleable ATM Architecture,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1994)*, vol. 2, pp. 1459-1463, 3-5 Aug. 1994.

- B. Alhalabi and M.A. Bayoumi, ‘‘A Hybrid Chip Set for Artificial Neural Network Systems,’’ *WCNN 1994*, June 1994, San Diego, CA.
- M. Altuwaijri, R. Ayoubi and M.A. Bayoumi, ‘‘Skeletonization of Arabic Characters using Neural Network Mapped on the MasPar,’’ *WCNN 1994*, June 1994, San Diego, CA.
- Q. M. Malluhi, M.A. Bayoumi, and T.R. Rao, ‘‘A Parallel Algorithm for Neural Computing,’’ *WCNN 1994*, June 1994, San Diego, CA.
- M.M. Altuwaijri and M.A. Bayoumi, ‘‘Arabic Text Recognition using Neural Networks,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1994)*, vol. 6, pp. 415-418, 30 May-2 June 1994, London.
- Ramakrishna N.A and M.A. Bayoumi, ‘‘Storage Allocation Strategies in Datapath Synthesis of ASICs,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1994)*, pp. 41-44, 30 May-2 June 1994, London.
- R.V. Cherabuddi and M.A. Bayoumi, ‘‘Simultaneous Partitioning, Scheduling and Allocation for Synthesis of Multi-Chip Modules,’’ *3rd International Workshop on Economics of Design, Test and Manufacturing*, pg. 129, 16-17 May 1994.
- A. Tyagi and M.A. Bayoumi, ‘‘ULSI Design-for-Manufacturability: A Yield Enhancement Approach,’’ *3rd International Workshop on Economics of Design, Test and Manufacturing*, pg. 80, 16-17 May 1994.
- R.V. Cherabuddi and M.A. Bayoumi, ‘‘Automated System Partitioning for Synthesis of Multi-Chip Modules,’’ *IEEE Great Lakes Symposium on VLSI (GLS 1994)*, pp. 15-20, 4-5 March 1994.
- A. Tyagi, M.A. Bayoumi and P. Manthravadi, ‘‘Yield Enhancement in the Routing Phase of Integrated Circuit Layout Synthesis,’’ *International Workshop on Wafer Scale Integration*, pp. 52-60, 19-21 Jan. 1994, San Francisco, CA.
- M.K. Kidambi, A. Tyagi, M.R. Madani and M.A. Bayoumi, ‘‘Parameterized Modeling of Open Circuit Critical Volume for Three-Dimensional Defects in VLSI Processing,’’ *VLSI Design 1994*, pp. 333-338, 5-8 Jan. 1994, Calcutta, India.

1993

- P. Srinivas, S. Varadarajan, V. Kalapatapu, and M. Bayoumi, ‘‘An Application Specific Architecture for Rate-distortion Optimized Motion Compensation,’’ *Computer Architectures for Machine Perception (CAMP 1993)*, pp. 362-369, 15-17 Dec. 1993.
- Q. M. Malluhi, M.A. Bayoumi and T.R.N. Rao, ‘‘An Efficient Mapping of Multilayer Perceptron with Backpropagation ANNs on Hypercubes,’’ *5th IEEE Symposium on Parallel and Distributed Processing*, pp. 368-375, 1-4 Dec. 1993.
- Q.M. Malluhi, M.A. Bayoumi and T.R.N. Rao, ‘‘An Application Specific Array Architecture for Feedforward with Backpropagation ANNS,’’ *International Conference on Application Specific Array Processors*, pp. 333-344, 25-27 Oct. 1993, Italy.
- S. Varadarajan, M.A. Bayoumi, ‘‘A VLSI Architecture for Rate-Distortion Optimized Motion Compensation Using Variable Size Blocks,’’ *Workshop on VLSI Signal Processing*, pp. 39-47, 20-22 Oct. 1993.
- R. V. Cherabuddi, N. A. Ramakrishna, M.A. Bayoumi, ‘‘Stochastic Evolution based Partitioning Technique for High Level Synthesis of MCMs,’’ *5th International Symposium on Circuits and Systems (ISCAS 1993)*, Sept. 1993, Singapore.

- S. Varadarajan, N.A. Ramakrishna, M.A. Bayoumi, ‘‘A Stochastic Evolution based Register Allocation Algorithm using Multiport Memories,’’ *Midwest Symposium on Circuits and Systems (MWSCAS 1993)*, pp. 472-475, 16-18 Aug. 1993.
- S. Varadarajan, P. Srinivas, V. Kalapatapu, and M.A. Bayoumi, ‘‘An Architecture for Rate Distortion Optimized Motion Estimation,’’ *Midwest Symposium on Circuits and Systems (MWSCAS 1993)*, vol. 2, pp. 954-957, 16-18 Aug. 1993.
- H. Kumar, R. Kalyan, M.A. Bayoumi, A. Tyagi, N. Ling, ‘‘Parallel Implementation of a Cut and Paste Maze Routing Algorithm,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1993)*, vol. 3, pp. 2035-2038, 3-6 May 1993.
- C. Zhao, M.A. Bayoumi, and M. Farooq, ‘‘A Multiprocessor-based "Universal" Interface for Multisensor-based Robotic System,’’ *IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing*, vol. 2, pp. 524-527, 19-21 May 1993.
- Q. M. Malluhi and M.A. Bayoumi, ‘‘On the Hierarchical Hypercube Interconnection Network,’’ *IEEE Parallel Processing Symposium (IPPS 1993)*, pp. 524-530, 13-16 April 1993.

1992

- M.A. Bayoumi, ‘‘VLSI Architectures for DSP Applications: Current Trends,’’ *IEEE Midwest Symposium on Circuits and Systems (MWSCAS 1992)*, pp. 150-153, 9-12 Aug. 1992.
- M.A. Bayoumi et al., ‘‘SDS: A Framework for the Design of DSP ASICs,’’ *IEEE International Conference on Signal Processing*, pp. 545-548, March 1992.
- Q.M. Malluhi and M.A. Bayoumi ‘‘Properties and Performance of the Hierarchical Hypercube,’’ *6th International Parallel Processing Symposium (IPPS 1992)*, pp. 47-50, 23-26 March 1992.
- M.A. Bayoumi and Ramakrishna N.A, ‘‘High Level Synthesis System for DSP Design,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1992)*, May 1992, pp. 172-175.
- Ramakrishna N. A, M.A. Bayoumi, and Subrata Dasgupta, ‘‘Design Process Management in a CAD Framework,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1992)*, May 1992, pp. 447-450.
- T. Madraswala and M.A. Bayoumi, ‘‘A Reconfigurable ANN Architecture,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1992)*, May 1992, pp. 1569-1572.
- B. Alhalabi, M.A. Bayoumi and Kimon Valavanis, ‘‘A General Purpose VLSI Chip for Robot Axis Motion Controller,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1992)*, May 1992, pp. 3005-3008.

1991

- G. Seetharaman, M.A. Bayoumi, K. Valavanis, M. Mulder, ‘‘VLSI Architecture for Stereo Image Sensors,’’ *Computer Architecture for Machine Perception Workshop (CAMP 1991)*, pp. 373-384, Dec. 1991.
- K. M. Elleithy and M.A. Bayoumi, ‘‘A Massively Parallel RNS Architecture,’’ *IEEE Asilomar Conference on Circuits, Computers, and Signal Processing*, pp. 408-412, 4-6 Nov. 1991.
- K. M. Elleithy and M.A. Bayoumi, ‘‘Formal Design of RNS Processors,’’ *International Conference on Circuits and Systems*, vol. 2, pp. 605-618, 16-17 June 1991, China.

- G. A. Jullien and M.A. Bayoumi, ‘‘A Review of VLSI Technologies in Digital Signal Processing,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1991)*, vol. 4, pp. 2347-2350 11-14 June 1991, Singapore.
- K.M. Elleithy and M.A. Bayoumi, ‘‘From Algorithms to Parallel Architectures: A Formal Approach,’’ *International Symposium on Parallel Processing*, pp. 348-363, 30 April-2 May 1991.
- S.R. Malladi, S.R. Myneni, P.V. Pothana and M.A. Bayoumi, ‘‘A High Speed FFT Processor,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 1991)*, vol. 3, pp. 1609-1612, 14-17 April 1991, Toronto.
- C. Hu, M.A. Bayoumi, B. Kearfott and Q. Yang, ‘‘A Parallelized Algorithm for the Reconditioned Interval Newton/Generalized Bisection Method,’’ *Fifth SIAM Conference on Parallel Processing for Scientific Computing*, 25-27 March 1991, Houston.
- A. Tyagi and M.A. Bayoumi, ‘‘A Generalized Poisson Based Model for Defect Spatial Distribution in WSI,’’ *IEEE International Conference of Wafer Scale Integration*, pp. 149-155, 29-31 Jan. 1991, San Francisco, CA.

1990

- P. Rao and M.A. Bayoumi, ‘‘An Algorithm Specific VLSI Parallel Architecture for Kalman Filter,’’ *VLSI Signal Processing IV*, pp. 264-273, Nov. 1990, San Diego, CA.
- K.M. Elleithy and M.A. Bayoumi, ‘‘A Formal Design Methodology for Parallel Architectures,’’ *International Conference of Application Specific Array Processors*, pp. 603-614, 5-7 Sept. 1990.
- K.M. Elleithy and M.A. Bayoumi, ‘‘Formal Synthesis of Parallel Architectures from Recursive Equations,’’ *International Conference on Parallel Processing*, Aug. 1990.
- A. Tyagi and M.A. Bayoumi, ‘‘Image Segmentation on a 2D Array Architecture,’’ *IEEE 10th International Conference on Pattern Recognition*, Atlantic City, 17-21 June 1990.
- A. Tyagi and M.A. Bayoumi, ‘‘Systolic Array Implementation of Image Segmentation by a Directed Split and Merge Procedure,’’ *10th International Conference on Pattern Recognition*, vol. 2, pp. 491-493, 16-21 June 1990.
- M.A. Bayoumi, J.L. Shah, and N. Ling, ‘‘Parallel Algorithms Prototyping: A Case Study,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1990)*, vol.4, pp. 3262-3266, 1-3 May 1990, New Orleans, LA.
- M.A. Bayoumi and P. Srinivasan, ‘‘Parallel Arithmetic: From Algebra to Architecture,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1990)*, vol. 4, pp. 2630-2633, 1-3 May 1990, New Orleans, LA.
- K.M. Elleithy and M.A. Bayoumi, ‘‘Synthesizing DSP Architectures from Behavioral Specifications: A Formal Approach,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1990)*, vol. 2, pp. 1131-1134, 1-3 May 1990.
- P. Rao and M.A. Bayoumi, ‘‘An Efficient VLSI Implementation of Real-Time Kalman Filter,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1990)*, vol. 3, pp. 2353-2356, 1-3 May 1990, New Orleans, LA.
- A. Tyagi and M.A. Bayoumi, ‘‘Yield Modeling for Fault Tolerant WSI Arrays,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1990)*, vol. 2, pp. 1616-1619, 1-3 May 1990.

- K.M. Elleithy and M.A. Bayoumi, ‘‘A Formal High Level Synthesis Approach for DSP Architectures,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 1990)*, vol. 2, pp. 897-900, 3-6 April 1990.
- K.M. Elleithy and M.A. Bayoumi, ‘‘A Formal Framework for Synthesis of Parallel Architectures,’’ *4th Annual Parallel Processing Symposium*, pp. 484-498, April 1990.
- K.M. Elleithy and M.A. Bayoumi, ‘‘A Framework for High Level Synthesis of Digital Architectures from μ-recursive Algorithms,’’ *ACM Computer Science Conference*, Washington D.C, Feb. 1990.

1989

- K.M. Elleithy, M.A. Bayoumi, and K.P. Lee, ‘‘θ(log n) Architectures for RNS Arithmetic Decoding,’’ *Symposium on Computer Arithmetic*,’’ pp. 202-209, 6-8 Sept. 1989.
- K.M. Elleithy and M.A. Bayoumi, ‘‘A θ(log n) Algorithm for Modulo Multiplication,’’ *IEEE International Midwest Symposium on Circuits and Systems (MSCAS 1989)*, pp. 353-356, 14-16 Aug. 1989.
- A. Tyagi and M.A. Bayoumi, ‘‘A Systolic Array for Image Implementation Using Split and Merge Procedure,’’ *Midwest Symposium on Circuits and Systems (MWSCAS 1989)*, pp. 345-348, 14-16 Aug. 1989, Urbana, IL.
- N. Ling and M.A. Bayoumi, ‘‘The Design and Implementation of Multidimensional Systolic Arrays for DSP Applications,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 1989)*, vol. 2, pp. 1142-1145, 23-26 May 1989, Glasgow.
- W. Bao and M.A. Bayoumi, ‘‘Systolic Architectures for High Order Correlation Artificial Neural Nets,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1989)*, vol. 2, pp. 1199-1202, 8-11 May 1989, Finland.
- K.P. Lee, M.A. Bayoumi, and K.M. Elleithy, ‘‘A Fast and Flexible Decoder Based on the Chinese Remainder Theorem,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1989)*, pp. 200-203, 8-11 May 1989, Finland.
- N. Ling and M.A. Bayoumi, ‘‘STA: A Tool for Systolic Array Reasoning,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1989)*, pp. 461-464, 8-11 May 1989, Finland.
- K.M. Elleithy, M.A. Bayoumi, and L. Delcambre, ‘‘A Systolic Machine for Relational Database and Hashing,’’ *Third Annual Parallel Processing Symposium*, pp. 621-635, March 1989.

1988

- N. Ling and M.A. Bayoumi, ‘‘The Specification and Verification of Systolic Arrays,’’ *IEEE Workshop on VLSI Signal Processing III*, pp. 435-446, Nov. 1988.
- S.R. Gupta and M.A. Bayoumi, ‘‘Concurrent Error Detection in Systolic Arrays for Real-time DSP Applications,’’ *IEEE Workshop on VLSI Signal Processing III*, pp. 470-482, Nov. 1988.
- M.A. Bayoumi, and K.A. Elleithy, ‘‘A Logic Programming Approach for DSP Architecture Design,’’ *22nd Asilomar Conference on Signals, Systems, and Computers*, pp. 753-757, 31 Oct.-2 Nov. 1988.
- N. Ling and M.A. Bayoumi, ‘‘Algorithms for High Speed Multi-Dimensional Arithmetic and DSP Systolic Arrays,’’ *International Conference on Parallel Processing (ICPP)*, pp. 367-374, Aug. 1988.

- N. Ling and M.A. Bayoumi, ‘‘A Testable NORA CMOS Serial-Parallel Multiplier,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1988)*, vol. 1, pp. 251-254, 7-9 June 1988, Finland.
- N. Ling and M.A. Bayoumi, ‘‘An Algorithm Transformation Technique for Multi-Dimensional DSP Systolic Arrays,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1988)*, vol. 3, pp. 2275-2278, 7-9 June 1988, Finland.
- S.R. Gupta and M.A. Bayoumi, ‘‘A Self-Testing Systolic Module for VLSI DSP Applications,’’ *IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 1517-1520, 7-9 June 1988, Finland.
- N.A. Ramakrishna and M.A. Bayoumi, ‘‘A Testable CMOS Signal Processor for Fast Fourier Transforms,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1988)*, 7-9 June 1988, Finland.
- M.A. Bayoumi and S.P. Popli, ‘‘A Reconfigurable VLSI Array for Reliability and Yield Enhancement,’’ *IEEE International Conference on Systolic Arrays*, pp. 631-642, 25-27 May 1988.
- M.A. Bayoumi, ‘‘Reliable Modulo Systolic Array for DSP Algorithms,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 1988)*, vol. 4, pp. 2076-2079, 11-14 April 1988, New York.
- N. Ling and M.A. Bayoumi, ‘‘Multi-Dimensional Systolic Networks for DSP Algorithms,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 1988)*, vol. 3, pp. 1922-1925, 11-14 April 1988, New York.
- R. Roy and M.A. Bayoumi, ‘‘A Fault-tolerant Bit-serial Array Structure for Digital Filters,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 1988)*, vol. 4, pp. 2100-2103, 11-14 April 1988, New York.
- M.A. Bayoumi and R. Roy, ‘‘Fault Tolerant Bit-Serial Systolic Arrays for DSP Applications,’’ *IEEE International Conference on ASSP*, pp. 2100-2103, April 1988.
- S.P. Popli and M.A. Bayoumi, ‘‘Fault Diagnosis and Reconfiguration For Reliable VLSI Arrays,’’ *Seventh IEEE Annual Phoenix Conference on Computers and Communications*, pp. 69-73, 16-18 March 1988.

1987

- M.A. Bayoumi and R. Roy, ‘‘A Bit-Serial Approach for Large Moduli-Based Architectures,’’ *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 1987, New York.
- N. Ling, M.A. Bayoumi, and K.S. Reddy, ‘‘VLSI Array Implementation of Modified Booth Algorithm,’’ *South Central Regional ACM Conference*, pp. 205-221, Nov. 1987, Lafayette, LA.
- R. Roy and M.A. Bayoumi, ‘‘A Fault-Tolerant Bit-Serial Array Structure for Digital Filters,’’ *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 1987)*, pp. 2100-2103, April 1987, New York.
- K.S. Reddy, M.A. Bayoumi, and V. Raghavan, ‘‘ A VLSI Parallel Architecture for Pattern Classification,’’ *South Central Regional ACM Conference*, pp. 189-204, Nov. 1987, Lafayette, LA.
- M.A. Bayoumi and S. R. Gupta, ‘‘A VLSI Implementation of Dadda Multiplier,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1987)*, Aug. 1987, New York.

- M.A. Bayoumi and J.C.H. Yang, ‘‘A Fault Tolerant Testable Module for Wafer Scale Integrated Systems,’’ *VLSI and Computers*, May 1987.
- M.A. Bayoumi, ‘‘VLSI PLA Structures For Residue Number Systems Arithmetic Implementation,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1987)*, pp. 132-135, May 1987.
- M.A. Bayoumi, ‘‘A Quadratic Residue Processor for Complex DSP Applications,’’ *IEEE International Conference in Acoustics, Speech, and Signal Processing (IASSP 1987)*, vol. 12, pp. 475-478, April 1987.
- M.A. Bayoumi, ‘‘Digital Filter VLSI Systolic Arrays Over Finite Fields For DSP Applications,’’ *6th IEEE Annual Phoenix Conference on Computers and Communications*, pp. 194-199, Feb. 1987.

1986

- M.A. Bayoumi,‘‘A Processing Based on Quadratic Residue Number System,’’ *IEEE Workshop on VLSI Signal Processing*, Nov. 1986. Also appeared in the *VLSI Signal Processing II*, pp. 200-211, IEEE press, 1986.
- M.A. Bayoumi, ‘‘A High Performance Modulo VLSI Signal Processor Architecture,’’ *20th IEEE Asilomar Conference on Signal, Systems and Computers*, Nov. 1986.
- M.A. Bayoumi, ‘‘VLSI Customized Arrays For RNS Based Structures,’’ *IEEE ICCD 1986*, pp. 510-513, Oct. 1986.
- M.A. Bayoumi, ‘‘VLSI Regular Layouts for RNS-Based Architectures,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1986)*, Aug. 1986.
- M.A. Bayoumi, N. Ramakrishna, S. Popli, ‘‘A High Performance Computational Unit for Fast Fourier Transform,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1986)*, pp. 640-643, Aug. 1986.
- M.A. Bayoumi, J. Yang, R. Roy, ‘‘A Fault-Tolerant Testable Multiplier for DSP Applications,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1986)*, pp. 637-639, Aug. 1986.
- S. Bandyopadhyay, G. A. Jullien, M.A. Bayoumi, ‘‘Systolic Arrays over Finite Rings with Applications to Digital Signal Processing,’’ *International Workshop on Systolic Arrays*, pp. 151-158, July 1986.
- M.A. Bayoumi, ‘‘Wafer Scale Integration for Generic RNS Structures,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1986)*, pp. 117-120, May 1986.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A VLSI Array for Computing the DFT Based on RNS,’’ *IEEE International Conference in Acoustics, Speech, and Signal Processing (ICASSP 1986)*, vol. 11, pp. 2147-2150, April 1986.

1985

- M.A. Bayoumi, ‘‘Implementation of RNS Multiplication in VLSI,’’ *19th Annual Asilomar Conference on Circuits, Systems and Computers*, pp. 48-52, 6-8 Nov. 1985.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A VLSI Implementation of RNS-Based Architectures,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1985)*, June 1985.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘Highly Parallel Architectures For DSP Algorithms,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1985)*, pp.

48-52, June 1985.

- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A VLSI Implementation of an FFT/NTT Computational Unit,’’ *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP 1985)*, pp. 192-195, April 1985.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘An Efficient VLSI Adder for DSP Architectures Based on RNS,’’ *IEEE International Conference in Acoustics, Speech, and Signal Processing (ICASSP 1985)*, pp. 1457-1460, April 1985.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘Area-Time Lower Bounds of VLSI Systems Based on RNS,’’ *16th Annual Pittsburgh Conference on Modeling and Simulation*, pp. 933-937, April 1985.

1984

- M.A. Bayoumi, G. A. Jullien and W. C. Miller, ‘‘An Array Implementation of Digital Filters,’’ *IEEE International Symposium on Circuits and Systems (MWSCAS 1984)*, pp. 1268-1271, May 1984.
- M.A. Bayoumi, G. A. Jullien and W. C. Miller, ‘‘Bit-Parallel Based Filters Using Residue Number System,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1984)*, pp. 304-307, June 1984.
- M.A. Bayoumi and J. J. Soltis, ‘‘An Analysis of a Microcomputer Based Image Processor,’’ *International Symposium on Mini and Microcomputers and their Applications*, pp. 75-78, June 1984.
- M.A. Bayoumi, G. A. Jullien and W. C. Miller, ‘‘I/O Strategies for Residue Number System Architectures for Digital Signal Processing Applications,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1984)*, pp. 1069-1072, May 1984.
- M.A. Bayoumi, M. Ahmadi and G. A. Jullien, ‘‘Near Real Time Image Processor Based on an Array of Multi-Microprocessor Systems,’’ *IEEE International Symposium on Circuits and Systems (ISCAS 1984)*, pp. 1272-1276, May 1984.
- M.A. Bayoumi, G. A. Jullien and W. C. Miller, ‘‘A Modular Implementation of Digital Signal Processing Architectures Using RNS,’’ *15th Annual Pittsburgh Conference on Modeling and Simulation*, pp. 1425-1430, April 1984.
- M.A. Bayoumi, G. A. Jullien and W. C. Miller, ‘‘A Systolic (VLSI) Array Using RNS for Digital Signal Processing Applications,’’ *ACM Computer Science Conference*, pp. 115-120, March 1984.

1983

- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘VLSI Implementation of RNS Modules and their Proposed Applications,’’ *21st Annual Allerton Conference*, pp. 1003-1013, Oct. 1983, Univ. of Illinois.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘A VLSI Implementation of an NTT Multiplier Using RNS for Digital Signal Processing Applications,’’ *2nd European Signal Processing Conference*, pp. 837-841, Sept. 1983.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘RNS Modules for VLSI Implementation of Digital Filters,’’ *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 1983)*, pp. 403-407, Aug. 1983.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘Models for VLSI Implementation of Residue Number System Arithmetic Modules,’’ *6th Symposium on Computer Arithmetic*, pp. 174-182,

June 1983.

- M.A. Bayoumi and M. Ahmadi, ‘‘A Multi-Microcomputer System for Image Enhancement,’’ *21st International Symposium on Mini and Microcomputers and their Applications*, pp. 52-56, May 1983.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘Modeling of Residue Number System Arithmetic Chips,’’ *14th Annual Pittsburgh Conference on Modeling and Simulation*, pp. 1361-1365, April 1983.
- M.A. Bayoumi, G.A. Jullien and W.C. Miller, ‘‘The Area-Time Complexity of a VLSI Residue Number System Arithmetic Unit,’’ *7th Conference on Information Sciences and Systems*, pp. 6-9, March 1983.