M. Hassan Najafi

Assistant Professor
Center for Advanced Computer Studies
School of Computing and Informatics
University of Louisiana at Lafayette
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RESEARCH INTERESTS

- Machine Learning
- Stochastic and Approximate Computing
- Performance Evaluation and Modeling
- High Performance Computing
- Digital Signal Processing
- Computer Architecture
- Fault Tolerant Design
- Low Power Design

POSITIONS

University of Louisiana (Lafayette, LA)
Assistant Professor of School of Computing and Informatics (CMIX) — Aug 2018 - Present

Endura Technologies LLC (San Diego, CA)
Consultant — May 2019 - Present

University of Minnesota-Twin Cities
Graduate Research Assistant in ARCTiC Lab — Aug 2014 - Jul 2018

University of Tehran
Graduate Research Assistant in Multicore Systems Lab — Sep 2012 - Jun 2014

TEACHING

• **Instructor**
CSCE 585 – VLSI Design (Grad.) — University of Louisiana – Fall'18, Fall'19
CSCE 583 - Computer Design and Implementation (Grad.) — University of Louisiana – Spring 2019

• **Teaching Assistant**
CE – Multicore Embedded Systems (Grad.) — University of Tehran – Spring 2013
CE – Advance Computer Architecture (Grad.) — University of Tehran – Fall 2012
CE – Embedded System Processing Elements (Grad.) — University of Tehran – Fall 2012-13
CE – Programming languages (Undergrad.) — University of Isfahan – Fall 2010

EDUCATION

PhD - University of Minnesota, Twin Cities — Aug 2014 - Jul 2018
Electrical and Electronics Engineering, GPA: 3.93/4.0
Thesis: New Views for Stochastic Computing: From Time-Encoding to Deterministic Processing
Advisor: David J. Lilja

MSc - University of Tehran, Tehran, Iran — Sep 2011 - Jun 2014
Computer Engineering—Computer Architecture, GPA: 3.94/4.0
Thesis: Exploiting Stochastic Computing for Error Resilient Processors
Advisor: Mostafa E. Salehi Nasab

BSc - University of Isfahan, Isfahan, Iran Sep 2006 - Jan 2011
Computer Engineering—Hardware
Thesis: Evaluation of Image Thresholding Algorithms
Advisor: Kamal Jamshidi

PUBLICATIONS

• **Patents**

[P8] **M. Hassan Najafi**, S. Rasoul Faraji, Bingzhe Li, David J. Lilja, and Kia Bazargan, "Resolution Splitting for Bit-Stream Processing", June 2019, Provisional U.S. Patent App. 62/864,798.

[P7] **M. Hassan Najafi**, David J. Lilja, and Marc Riedel, "Low-discrepancy Deterministic Bit-stream Processing Using Sobol Sequences", June 2019, Provisional U.S. Patent App. 62/864,807.

[P6] Bingzhe Li, **M. Hassan Najafi**, and David J. Lilja, "Low-Cost Stochastic Hybrid Multiplier for Quantized Neural Networks", March 2019, Provisional U.S. Patent App. 62/817,343.

[P5] **M. Hassan Najafi**, David J. Lilja, Marc Riedel, and Kia Bazargan, "Sorting Networks using Unary Pro-cessing", Nov 2018, U.S. Patent App. 16/674488, Pending.

[P4] Karen Khatamifard, **M. Hassan Najafi**, Ali Ghoreyshi, Ulya Karpuzcu, David J. Lilja, "Stochastic Computing with Analog Memory", September 2018, Provisional U.S. Patent App. 62/735584.

[P3] **M. Hassan Najafi** and David J. Lilja, "High Quality Down-Sampling for Deterministic Bit-Stream Computing", Mar 2018, U.S. Patent App. 16/352,933, Pending.

[P2] **M. Hassan Najafi**, S Jamali-Zavareh, D. J. Lilja, M. Riedel, K. Bazargan, and R. Harjani, "Stochastic Computation Using Pulse Width Modulated Signals", Jan 2018, U.S. Patent App. 15/869453, Pending.

[P1] David J. Lilja, **M. Hassan Najafi**, Marc Riedel and Kia Bazargan, "Polysynchronous Stochastic Circuits", Granted U.S. Patent 10,520,975 B2, Date of Patent: Dec 31 2019.

• **Book Chapters**

[B1] **M. Hassan Najafi**, S. R. Faraji, B. Li, D. J. Lilja and K. Bazargan, "Stochastic-Binary Convolutional Neural Networks with Deterministic Bit-streams," in Hardware Architectures for Deep Learning, Publisher: IET, April 2020.

• **Journals**

[J10] **M. Hassan Najafi**, D. Jenson, M. Riedel and D. J. Lilja, "Performing Stochastic Computation Deterministically," in IEEE Tran. on Very Large Scale Integration (VLSI) Systems, Dec 2019.

[J9] B. Li, **M. Hassan Najafi**, and David Lilja, "Low-Cost Stochastic Hybrid Multiplier for Quantized Neural Networks," in ACM Journal on Emerging Technologies in Computing Systems (JETC), 2019.

[J8] **M. Hassan Najafi**, D. J. Lilja, M. D. Riedel and K. Bazargan, "Low-Cost Sorting Network Circuits Using Unary Processing," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Aug 2018.

[J7] S. K. Khatamifard, **M. Hassan Najafi**, A. Ghoreyshi, U. R. Karpuzcu and D. J. Lilja, "On Memory System Design for Stochastic Computing," in IEEE Computer Architecture Letters, July-Dec. 2018.

[J6] **M. Hassan Najafi** and D. Lilja, "High Quality Down-Sampling for Deterministic Approaches to Stochastic Computing," in IEEE Transactions on Emerging Topics in Computing (TETC), 2018.

[J5] **M. Hassan Najafi**, S. Jamali-Zavareh, D. J. Lilja, M. D. Riedel, K. Bazargan and R. Harjani, "An Overview of Time-Based Computing with Stochastic Constructs," in IEEE Micro, Dec. 2017.

[J4] **M. Hassan Najafi**, D. J. Lilja, M. D. Riedel and K. Bazargan,"Polysynchronous Clocking: Exploiting the Skew Tolerance of Stochastic Circuits," in IEEE Tran. on Computers, Oct. 2017.

[J3] **M. Hassan Najafi**, P. Li, D. J. Lilja, W. Qian, K. Bazargan, and M. Riedel. 2017. "A Reconfigurable Architecture with Sequential Logic-Based Stochastic Computing". ACM Journal on Emerging Technologies in Computing Systems (JETC). June 2017.

[J2] **M. Hassan Najafi**, S. Jamali-Zavareh, D. J. Lilja, M. D. Riedel, K. Bazargan and R. Harjani, "Time-Encoded Values for Highly Efficient Stochastic Circuits," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, May 2017.

[J1] **M. Hassan Najafi** and M. E. Salehi, "A Fast Fault-Tolerant Architecture for Sauvola Local Image Thresholding Algorithm Using Stochastic Computing," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Feb. 2016

• **Conferences**

[C28] Sina Asadi and **M. Hassan Najafi**, "Accelerating Deterministic Stochastic Computing with Context-Aware Bit-stream Generator," The 30th ACM Great Lakes Symposium on VLSI (GLSVLSI), Beijing, China, May 2020.

[C27] **M. Hassan Najafi**, D. Jenson, M. Riedel and D. J. Lilja, "Performing Stochastic Computation Deterministically," The 2020 IEEE International Symposium of Circuits and Systems (ISCAS), Seville, Spain, May 2020.

[C26] R. Hojabr, K. Givaki, K. Pourahmadi, P. Nooralinejad, A. Khonsari, D. Rahmati, **M. Hassan Najafi**, "TaxoNN: a Light-Weight Accelerator for Deep Neural Network Training," The 2020 IEEE International Symposium of Circuits and Systems (ISCAS), Seville, Spain, May 2020.

[C25] Mohsen Riahi Alam, **M. Hassan Najafi** and Nima TaheriNejad, "Exact In-Memory Multiplication Based on Deterministic Stochastic Computing," The 2020 IEEE International Symposium of Circuits and Systems (ISCAS), Seville, Spain, May 2020.

[C24] A. H. Jalilvand, **M. Hassan Najafi** and M. Fazeli, "Fuzzy-Logic Using Unary Bit-Stream Processing," The 2020 IEEE International Symposium of Circuits and Systems (ISCAS), Seville, Spain, May 2020.

[C23] **M. Hassan Najafi**, S. Rasoul Faraji, K. Bazargan and David J. Lilja, "Energy-Efficient Pulse-Based Convolution for Near-Sensor Processing," The 2020 IEEE International Symposium of Circuits and Systems (ISCAS), Seville, Spain, May 2020.

[C22] S. Gupta, M. Imani, J. Sim, A. Huang, F. Wu, **M. Hassan Najafi** and T. Rosing, "SCRIMP: A General Stochastic Computing Architecture using ReRAM in-Memory Processing," The 2020 Design, Automation, and Test in Europe (DATE), Grenoble, France, 2020.

[C21] S. Asadi and **M. Hassan Najafi**, "Context-Aware Number Generator for Deterministic Bit-stream Computing," 2019 IEEE 30th International Conference on Application-specific Systems, Architectures and Processors (ASAP), New York, NY, July 2019.

[C20] K. Givaki, R. Hojabr, **M. Hassan Najafi**, A. Khonsari, M. H. Gholamrezayi, S. Gorgin and D. Rahmati, "Using Residue Number Systems to Accelerate Deterministic Bit-stream Multiplication," 2019 IEEE 30th International Conference on Application-specific Systems, Architectures and Processors (ASAP), New York, NY, July 2019.

[C19] **M. Hassan Najafi**, S. Rasoul Faraji, K. Bazargan and D. J. Lilja, "Energy-Efficient Near-Sensor Convolution using Pulsed Unary Processing," 2019 IEEE 30th International Conference on Application-specific Systems, Architectures and Processors (ASAP), New York, NY, July 2019.

[C18] B. Li, Jiaxi Hu, **M. Hassan Najafi**, S. Koester, and D. Lilja, "Low Cost Hybrid Spin-CMOS Compressor for Stochastic Neural Networks", The 29th ACM Great Lakes Symposium on VLSI (GLSVLSI), Washington, D.C., May 2019.

[C17] R. Hojabr, K. Givaki, SM R. Tayaranian, P. Esfahanian, A. Khonsari, D. Rahmati, and **M. Hassan Najafi**, "SkippyNN: An Embedded Stochastic-Computing Accelerator for Convolutional Neural Networks ", The 56th Design Automation Conference (DAC), Las Vegas, NV, 2019.

[C16] ***M. Hassan Najafi**, *S. R. Faraji, B. Li, D. J. Lilja, and K. Bazargan, "Accelerating Deterministic Bit-Stream Computing with Resolution Splitting," 2019 20th International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, 2019. (*contributed equally).

[C15] *S. R. Faraji, ***M. Hassan Najafi**, B. Li, K. Bazargan, and D. Lilja, Energy-Efficient Convolutional Neural Networks with Deterministic Bit-Stream Processing, The 2019 Design, Automation, and Test in Europe (DATE), Florence, Italy, 2019. (*contributed equally)

[C14] **M. Hassan Najafi**, D. J. Lilja, and M. Riedel. Deterministic methods for stochastic computing using low-discrepancy sequences. In Proceedings of the International Conference on Computer-Aided Design (ICCAD), San Diego, CA, Nov 2018.

[C13] B. Li, **M. Hassan Najafi**, B. Yuan and D. J. Lilja, "Quantized neural networks with new stochastic multipliers," 2018 19th International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, 2018, pp. 376-382.

[C12] **M. Hassan Najafi** and D. J. Lilja, "High Quality Down-Sampling for Deterministic Approaches to Stochastic Computing," 2017 IEEE International Conference on Computer Design (ICCD), Boston, MA, 2017.

[C11] **M. Hassan Najafi**, D. J. Lilja, M. Riedel and K. Bazargan, "Power and Area Efficient Sorting Networks Using Unary Processing," 2017 IEEE International Conference on Computer Design (ICCD), Boston, MA, 2017, pp. 125-128.

[C10] **M. Hassan Najafi**, S. Jamali-Zavareh, D. Lilja, M. Riedel, K. Bazargan, and R. Harjani, "Time-Encoded Values for Highly Efficient Stochastic Circuits," ISCAS 2017.

[C9] S. K. Khatamifard, **M. Hassan Najafi**, A. Ghoreyshi, U. Karpuzcu, D. J. Lilja, "StochMem: Towards Seamless Stochastic Computing Systems with Analog Memories", (WIP) DAC 2017.

[C8] **M. Hassan Najafi** and D. J. Lilja, "High-speed stochastic circuits using synchronous analog pulses," 2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC), Chiba, 2017, pp. 481-487.

[C7] **M. Hassan Najafi**, D. J. Lilja, M. Riedel and K. Bazargan, "Polysynchronous stochastic circuits," 2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC), Macau, 2016, pp. 492-498.

[C6] **M. Hassan Najafi**, D. J. Lilja, M. Riedel, and K. Bazargan, "Quantifying the Benefits of Stochastic Com-putation with Polysynchronous Clocking", (WIP) DAC 2016.

[C5] Bingzhe Li, **M. Hassan Najafi**, and David J. Lilja. 2016. Using Stochastic Computing to Reduce the Hardware Requirements for a Restricted Boltzmann Machine Classifier. In Proceedings of the 2016 ACM/SIGDA International Symp. on Field-Programmable Gate Arrays (FPGA). pp 36-41.

[C4] **M. Hassan Najafi**, A. Murali, D. J. Lilja and J. Sartori, "GPU-Accelerated Nick Local Image Thresholding Algorithm," 2015 IEEE 21st International Conference on Parallel and Distributed Systems (ICPADS), Melbourne, VIC, 2015, pp. 576-584.

[C3] B. Li, **M. Hassan Najafi** and D. J. Lilja, "An FPGA implementation of a Restricted Boltzmann Machine classifier using stochastic bit streams," 2015 IEEE 26th International Conference on Application-specific Systems, Architectures and Processors (ASAP), Toronto, ON, 2015, pp. 68-69.

[C2] M. Ranjbar, M. E. Salehi and **M. Hassan Najafi**, "Using stochastic architectures for edge detection algorithms," 2015 23rd Iranian Conf. on Electrical Engineering, Tehran, 2015, pp. 723-728.

[C1] **M. Hassan Najafi** and M. E. Salehi, "Exploring the design space for area-efficient embedded VLIW packet processing engine," 2013 21st Iranian Conference on Electrical Engineering (ICEE), Mashhad, 2013, pp. 1-6.

• **Workshops**

[W7] M. Riahi Alam, **M. Hassan Najafi** and N. TaheriNejad, "Exact Stochastic Computing Multiplication in Memristive Memory", 2020 Computation-In-Memory: from Device to Applications Workshop (CIMW), Grenoble, France, March 2020.

[W6] S. Asadi and **M. Hassan Najafi**, "Context-Aware Bit-stream Generator for Deterministic Unary Processing", 1st ISCA Workshop on Unary Computing (WUC), Phoenix, AZ, June 2019.

[W5] A. H. Jalilvand, **M. Hassan Najafi** and M. Fazeli, "Fuzzy-logic Processing using Unary Bit-Streams" *(invited)*, 1st ISCA Workshop on Unary Computing (WUC), Phoenix, AZ, June 2019.

[W4] K. Givaki, R. Hojabr, **M. Hassan Najafi**, A. Khonsari, S. Gorgin and Dara Rahmati, "Accelerating Unary Bit-Stream Processing Using Residue Numbers", 1st ISCA Workshop on Unary Computing (WUC), Phoenix, AZ, June 2019.

[W3] **M. Hassan Najafi**, S. Rasoul Faraji, Kia Bazargan and David J. Lilja, "Energy-Efficient Pulse-based Convolution Engine for Near-Sensor Processing" *(invited)*, 1st ISCA Workshop on Unary Computing (WUC), Phoenix, AZ, June 2019.

[W2] **M. Hassan Najafi**, D. J. Lilja, and M. Riedel, "Fast-Converging, Scalable, Deterministic Bit-Stream Computing using Low-Discrepancy Sequences", 27th International Workshop on Logic & Synthesis (IWLS), San Francisco, CA, 2018.

[W1] ***M. Hassan Najafi**, *S. R. Faraji, B. Li, D. J. Lilja, and K. Bazargan, "Using Resolution Splitting to Enhance Performance of Deterministic Bit-Stream Computing", 27th International Workshop on Logic & Synthesis (IWLS), San Francisco, CA, 2018. (*contributed equally).

AWARDS AND HONORS

• **EDAA Outstanding Dissertation Award (March 2019)**
My Ph.D. dissertation was selected to receive the 2018 Outstanding Dissertation Award in the area of "New Directions in Logic, Physical Design and CAD for Analog/Mixed-signal, Nano-Scale and Emerging Technologies" from the European Design and Automation Association (EDAA)

• **Best Poster Award in Design Automation Conference (DAC) PhD Forum (June 2019)**
My Ph.D. dissertation received the Best Poster Award at the 2019 Design Automation Conference PhD Forum among 58 accepted dissertations.

• **Best Paper Award in International Conference on Computer Design (ICCD)(Nov 2017)**
My paper on high-quality down-sampling of deterministic approaches to SC selected as the Best Paper of ICCD 2017 and was among the top ranked ICCD papers to be published in the IEEE TETC.

• **Doctoral Dissertation Fellowship (University of Minnesota, 2017)**
This fellowship is awarded to outstanding doctoral students. It includes a nine-month stipend of $25,000 plus tuition and $1,000 Conference Presentation Grant.

• **ECE Department Fellowship (University of Minnesota, 2014)**
This fellowship is awarded to new graduate students with outstanding academic background. It includes tuition and stipend for nine months with a total salary of $7,144.80.

• **IEEE Transaction on Computers Feature Paper of Month (Oct 2017)**
My paper "Polysynchronous Clocking: Exploiting the Skew Tolerance of Stochastic Circuits" selected by the Editor-in-chief of IEEE Transaction on Computers in collaboration with other experts.

• **IEEE Intern. Conf. on Computer Design (ICCD) Student Travel Grant (Nov 2017)**
This award includes $400 student travel award for attending ICCD-2017, Boston, MA, USA.

• **Council of Graduate Students Conf. Travel Award (Univ. of Minnesota, May 2017)**
This award includes $780 conference travel award for attending ISCAS-2017, Baltimore, MD, USA.

• **IEEE Computer Society TCPP Student Travel Award (Dec 2015)**
This award includes $400 student travel award for attending ICPADS-2015, Melbourne, Australia.

• **Ranked 1st among all students of Master of Computer Engineering-Computer Architecture, 2011 beginners (University of Tehran, 2011-2013)**

INVITED TALKS

[T7] "From Unary to Low-Discrepancy: Deterministic Bit-streams Revolutionize Stochastic Computing"
Workshop on Stochastic Computing for Neuromorphic Architectures (SCONA2020),
Grenoble, France, March 2020.

[T6] "Energy Efficient Convolutional Neural Networks Using Stochastic Computing"
University of Louisiana at Lafayette, Lafayette, Feb. 7, 2020

[T5] "Energy Efficient Convolutional Neural Networks Using Stochastic Computing"
Institute for Research in Fundamental Sciences (IPM), Tehran, IRAN, Dec. 19, 2019

[T4] "Performing Stochastic Computation Deterministically"
University of Louisiana at Lafayette, Lafayette, LA, Feb. 15, 2019

[T3] "Time-Based Computing with Stochastic Constructs"
Institute for Research in Fundamental Sciences (IPM), Tehran, IRAN, Jan. 3, 2019

[T2] "Fast-Converging Deterministic Methods for Stochastic Computing"
University of Tehran, Tehran, IRAN, Jan. 2, 2019

[T1] "Time-Based Computing with Stochastic Constructs"
University of Louisiana at Lafayette, April, 2018

ADVISING AND MENTORING

• **Doctoral Student**

Sina Asadi (Jan 2019–), University of Louisiana

Boisy Pitre (Sep 2018–), University of Louisiana

• **Visiting Research Scholar**

Mohsen Riahi Alam (May 2019–), University of Louisiana

Peter Schober (Sep 2019–Dec 2019), University of Louisiana

• **Master's Student**

Deepak Srivatsav Sridharan (Spring and Summer 2018), University of Minnesota
Project: development of low-cost parallel Sobol sequence generators for stochastic circuits

Yuejun Ma (Spring and Summer 2018), University of Minnesota
Project: development of a stochastic computing-based speech recognition system

SKILLS

Programming Languages: Python, C, C++, C#, CUDA C GPU Programming, Java, Visual Basic, TCL and BASH scripting
Hardware description language: Verilog
Tools: Xilinx Design suite, Altera Quartus, Synopsys Design Compiler, Cadence SoC Encounter, HSpice, LEdit, SEdit, ModelSim, Matlab, Lingo, Espresso, and Visual Studio
Microarchitectural Simulator/Tools: MARSSx86, Multi2Sim, SimpleScalar, Vex, BookSim

PROFESSIONAL SERVICE

• **Journal Paper Refereeing**
ACM Transactions on Design Automation of Electronic Systems (TODAES) 2019
IEEE Transactions on Very Large-Scale Integration Systems (TVLSI) 2015-2019
IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) 2018
ACM Transactions on Architecture and Code Optimization (TACO) 2018-2019
IEEE Transactions on Multi-Scale Computing Systems (TMSCS) 2016
ACM Transactions on Embedded Computing Systems (TECS) 2016
IEEE Transaction on Computers (TC) 2017-2019
IEEE Transaction on Nuclear Science (TNC) 2016
Mathematical Problems in Engineering, 2017
IET Computers & Digital Techniques 2018
IEEE Embedded Systems Letters 2017
IEEE Micro 2018-2019
IEEE Acess 2019

• **Conference and Workshop Paper Refereeing**
ACM/IEEE International Symposium on Computer Architecture (ISCA) 2020
ACM/IEEE Design Automation Conference (DAC) 2019-2020
International Conference on Supercomputing (ICS) 2017
International Conference on Parallel Architectures and Compilation Techniques (PACT) 2017
International workshop on Re-Emergence of Vector Architectures (REV-A) 2017
International workshop on Non-Volatile Memories (NVMW) 2018

• **Session Chair**
The 2020 IEEE International Symposium of Circuits and Systems (ISCAS)

• **Review Panel**
Natural Sciences and Engineering Research Council of Canada (NSERC) 2019

REFERENCES

- **David J Lilja**
  Louis John Schnell Professor of Electrical and Computer Engineering
  University of Minnesota
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- **Marc D. Riedel**
  Associate Professor of Electrical and Computer Engineering
  University of Minnesota
  ✉ mriedel@umn.edu ☎ +1 (612) 625 6086
- **Kia Bazargan**
  Associate Professor of Electrical and Computer Engineering
  University of Minnesota
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